University of Alberta

DESIGN AND IMPLEMENTATION OF NOVEL CURRENT CONTROL TECHNIQUES FOR SINGLE AND THREE PHASE PWM BOOST RECTIFIERS

By

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A thesis

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Abstract

A novel unipolar pulse width modulated (PWM) current control technique is examined for single and three phase unity fundamental power factor (UFPF) utility rectifier topologies. A comparison between a novel PWM averaging current control technique and the proportional-integral (PI) current control schemes for single and three phase utility rectifiers is presented. The behaviour of the proposed current control scheme is analyzed under both single phase and three phase operating conditions.

An investigation through comprehensive single and three phase simulations indicates the advantages of the proposed current control technique over the PI control scheme, such as stable steady-state operation, quick transient responses with minimal overshoots, and an inherent tolerance to system disturbances such as DC offsets. Analog realization of the current controllers are developed and implemented based on theoretical and simulation results. The experimental results demonstrate excellent performance of the controllers and present good agreement between the simulations and experiments.

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Nouman Ahmed Noor

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Nomenclature

f_{20dB}	20dB attenuation frequency of the 2nd order lowpass Butterworth filter ($f_{20dB} = 3.14 * f_{3dB}$)
f_{3dB}	3dB attenuation frequency of the 2nd order lowpass Butterworth filter
L_s	Supply inductance
ΔI_s	Linear ramp in the inductor current
$\Delta I_{s,\,max}$	Maximum peak-peak current ripple
POL	Polarity signal of the supply voltage
V_{DC}	DC Link voltage
E_{fbk}	DC link voltage feedback signal
E_{fbkF}	Filtered DC link voltage feedback signal
E_{ref}	Voltage reference signal for the DC link voltage
E_{error}	DC link voltage error signal
i_{fbk}	A feedback signal representing the line current
i_{error}	Steady-state current error signal (1V = 1A)
i_{errorF}	Filtered steady-state current error signal (1V = 1A)
v_{ref}	Voltage reference signal for PWM modulation
Δv_{ref}	The peak-to-peak ripple in the input v_{ref}
v_{pwm}	PWM voltage signal
$v_{pwm,\,ave}$	The average of the PWM voltage
m_n	Modulation depth signals for three phase where $n = a, b, c$
$m_{n,\,ideal}$	The ideal modulation depth signal for three phase where $n = a, b, c$
PWM	Pulse Width Modulation
$SPWM$	Sinusoidal Pulse Width Modulation
$PD\ PWM$	Phase disposition PWM

S	Switching signal applied to the power electronics
v_c	Triangle wave signal
v_{cp}	Positive carrier signal in PD PWM
v_{cn}	Negative carrier signal in PD PWM
PWM_p	PWM signal generated by v_{cp}
PWM_n	PWM signal generated by v_{cn}
PI	Proportional-integral controller
h	Hysteresis band
$S\&H$	Sample and Hold
K_i	Integral gain of the PI controller
K_I	Proportional gain for the current error signal
K_p	Proportional gain for the current error signals ($K_p = 10*K_I$)
THD	Total Harmonic Distortion (typically given in percent)
$UFPF$	Unity Fundamental Power Factor
GTO	Gate Turn-off Thyristor
$IGBT$	Insulated Gate Bipolar Transistor
UPS	Uninterruptable Power Supply
PLL	Phase Locked Loop

Chapter 1 Introduction

The concept of harmonic distortion is not unique in today's industrial processes. At the present, harmonic distortions constitute one of the main concerns for engineers in several stages of energy utilization within the power industry [1]. The increasing use of non-linear loads in industrial processes is keeping harmonic distortions in the distribution networks on the rise. Thus, distortions caused by harmonics in utility power supplies and the deterioration of power factors due to non-linear loads is considered to be a form of electrical pollution which can have dire consequence on industrial equipment and processes. Such effects can range from spurious operation of equipment to reduced efficiency of the entire power system.

The increasing use of power converters in industrial processes has made power converters the most widespread source of harmonic distortions in distribution systems. Power converters, such as voltage rectifiers, find wide applications in industrial processes such variable speed drives, uninterruptible power supplies (UPS), static compensators (STATCOM), and active power filters. Recent studies indicate that pulse width modulated (PWM) rectifiers offer a better alternative to conventional diode rectifiers with respect to harmonic mitigation; PWM rectifiers exhibit lower input current total harmonic distortion (THD) and output voltage THD compared to diode rectifiers [2]. The change towards the use of PWM rectifiers in industrial processes is largely due to IEEE 519-1992 recommended practice for harmonic regulation, which dictates a limit of 5% current THD for a load connected to a weak utility system [1]. In reality, an input current THD of 5% is often unachievable at a point of common coupling due the varying nature of linear and non-linear loads; as such, the limit set by IEEE 519-1992 is viewed by many in the industry as a desirable goal as opposed to a required operating condition. Consequently, the recommended practice laid out by IEEE 519-1992 is typically used for guidance in the design of power systems with non-linear loads.

In order to achieve low THD and a unity fundamental power factor (UFPF), an effective control scheme with fast transient response and accurate tracking is required. Current control techniques such as hysteresis current control, ramp comparison control, predictive and deadbeat controls, fuzzy and neural logic controls have provided an

effective means of controlling PWM rectifiers. This chapter provides a brief introduction to single phase and three phase power rectifiers. The concept of harmonic pollution as well as the sources and effects of harmonic distortion are also introduced. Furthermore, the general concept of PWM current control of power rectifiers is also discussed.

1.1 Current Control Fundamentals and Research Motivation

The performance of a PWM power rectifier is highly dependent on the quality of the control scheme being utilized. As a result, control of PWM rectifiers has become one of the most important subjects in power electronics. The fundamental principle behind current control is the same regardless of which control scheme is used. In essence, current controllers minimize the error between the supply and reference currents while determining the proper switching states for the PWM converter. Figure 1.1 illustrates a basic block diagram which is common to most PWM current controllers in existence today.

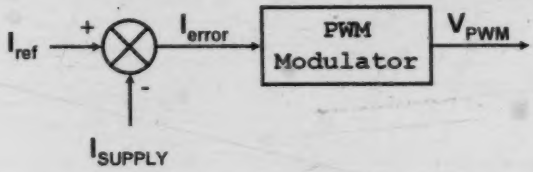
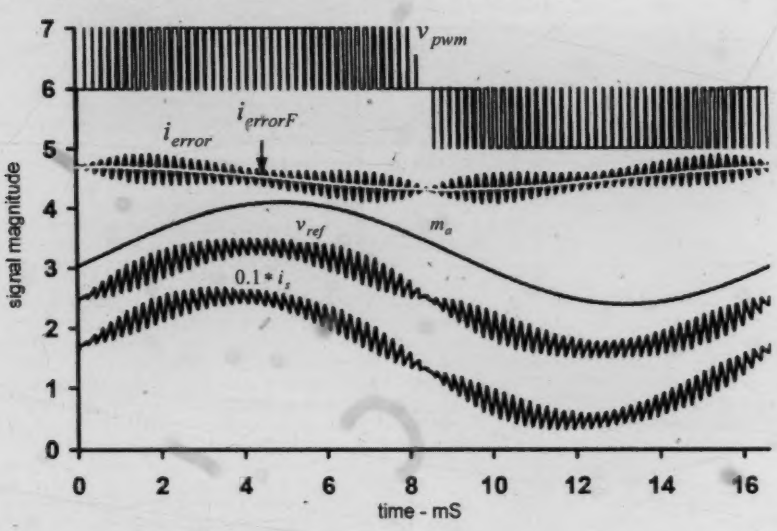


Figure 1.1: PWM current controller

The difference between the actual measured current and its respective reference current yields a current error signal I_{error}. A desired PWM modulator minimizes this current error and generates the switching pattern for the switching devices. Thus, for a PWM rectifier, the current controller forces the line current to follow the reference signals while drawing sufficient current to satisfy the load demand.

Figure 1.2 shows basic current control waveforms for a single phase PWM rectifier using unipolar PWM. A typical current error waveform consists of a high frequency ripple and a steady-state current error component. The high frequency ripple is directly related to the ramping of the supply current across the line inductor and is independent of the control scheme; as a result, a current controller cannot directly influence the magnitude of the high frequency ripple. The filtered current error signal i_{errorF} represents the average of the current error (or the steady-state current error between

the reference and the line currents) and is actively minimized by the controller; thus allowing the high frequency component to be centred on zero.



f_c = 5 kHz, L_s = 2.25 mH (5%), $I_{s,pk}$ = 10 A, V_s = 120 V, f_s = 60 Hz

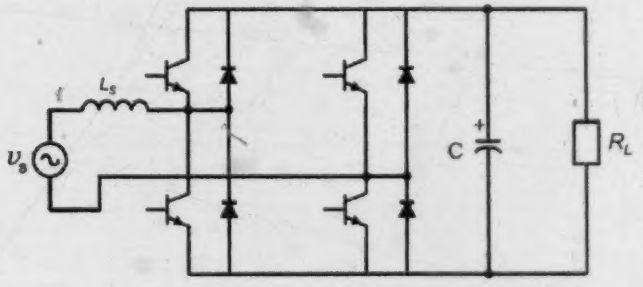
Figure 1.2: Waveforms associated with a basic current controller

Existing current control strategies can achieve low harmonic distortions while maintaining a unity fundamental power factor; however, the performance and complexity of the control is highly dependent on the scheme being utilized. Each control strategy presents its own unique set of advantages and disadvantages. For example, fixed-band hysteresis current controllers are simple to implement and exhibit little or no tracking error while maintaining high system dynamics; however, extra complexity is often required in order to obtain a constant switching frequency [3]. Ramp comparison current control techniques can provide a constant switching frequency but require extra complexity to obtain little or no tracking error [4, 5]. Predictive and deadbeat current control schemes are excellent at forcing small current errors to minimize tracking error; however, these control methods are dependant on a microprocessor for computational needs which adds to the complexity and cost of the current controller [6]. The proposed current control scheme for single and three phase PWM rectifiers utilizes the advantages of both fixed-band hysteresis-based current control and carrier-based fixed frequency current control schemes.

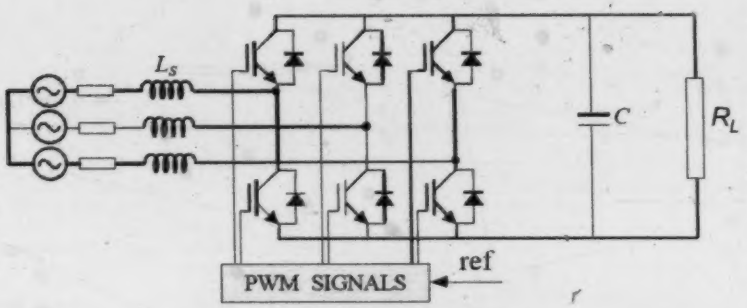
This thesis is focused on the design and implementation of a novel unipolar PWM current control technique for single and three phase unity fundamental power factor utility rectifier topologies. The proposed current control technique is capable of providing a zero average current error while maintaining a constant switching frequency. The behaviour of the proposed current control scheme is analyzed under both single phase and three phase operating conditions. Simulation and experimental results are compared and discussed to evaluate the proposed current control scheme. The proposed PWM current control technique presents a simple and low cost solution to controlling single and three phase UFPF utility rectifiers.

1.2 Fundamentals of PWM Rectifiers

The main disadvantages of the conventional uncontrolled diode rectifiers are that they produce a lagging displacement factor with respect to the supply voltage while generating large amount of input current harmonics. These aspects have a negative influence on both the power factor and power quality. An actively controlled rectifier utilizing forced commutated devices such as gate-turn off thyristors (GTO) and insulated bipolar transistors (IGBTs) can significantly improve the input power factor and reduce the harmonic distortions. The most effective strategy for controlling a rectifier via forced commutation is pulse width modulation (PWM) [2, 6, 8]. PWM rectifiers can be half-wave or full-wave in nature; however, full-wave PWM rectifiers are more commonly used in industrial applications. Figure 1.3 shows the basic topology for single and three phase force-commutated PWM rectifiers.



(a) Single phase PWM bridge rectifier



(b) Three phase PWM bridge rectifier

Figure 1.3: Bridge topology for single and three phase pwm rectifiers

In PWM control, the rectifier switches are turned on and off several times during a half-cycle and the output voltage is controlled by varying the pulse widths. The lower order harmonics can be significantly reduced or even eliminated by selecting the number of pulses per half-cycle. However, increasing the number of pulses also increases the magnitude of higher order harmonics, which are easily filtered out [2, 6]. There are different methods of varying the pulse widths but the most common one is the sinusoidal pulse width modulation (SPWM) technique. Pulse width modulation is generally obtained by comparing a modulation reference signal with a triangular carrier signal (figure 1.4). In SPWM, this modulation reference signal is sinusoidal; the pulse widths are varied by changing the amplitude of the sine wave reference signal or the modulation index from 0 to 1.

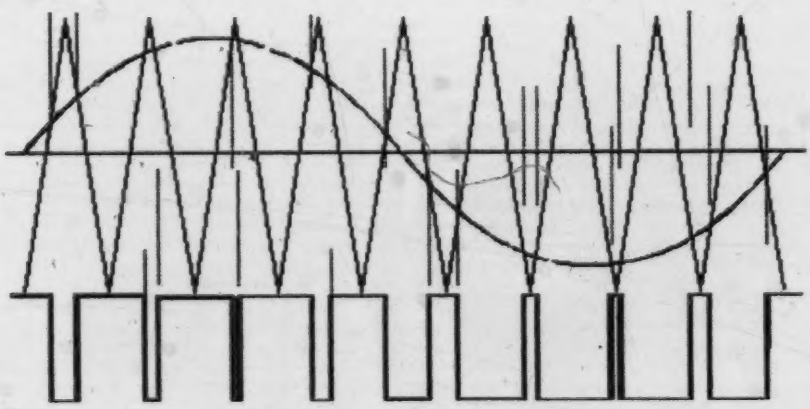


Figure 1.4: SPWM modulation

The modulation index is defined as the amplitude ratio of the modulation reference signal and the triangular carrier signal.

$$m_a = \frac{A_{ref}}{Ac} \tag{1.1}$$

For unmodulated pulses (M=0), the harmonic spectrum of the output voltage displays a strong harmonic component at the switching frequency of the PWM rectifier. As the modulation index increases, the harmonic component at the switching frequency decreases and the low frequency component at the fundamental frequency (i.e. at the frequency of the modulation reference signal) increases. However, the modulation index can only be increased until the widest pulse in the switching pattern fits the whole switching period. This is only possible when the amplitudes of the modulation reference signal and the triangular carrier signal are equal ($m_a = 1$). Any increase in the modulation index beyond $m_a = 1$ will cause a loss of the linear relationship between the modulation index and the average PWM output signal thus resulting in the distortion of the fundamental frequency waveform.

Since PWM can control both the active power and reactive power, PWM rectifiers can be used for power factor (PF) correction. The AC current waveforms can also be maintained almost sinusoidal via various current control techniques, which reduce harmonic contamination of the mains voltage supply. Recent years have seen a drive towards the use of PWM boost rectifiers in single and three phase industrial applications. Much like bridge type PWM rectifiers, boost rectifiers are capable of providing a unity fundamental power factor while maintaining a near sinusoidal supply current. Figures 1.5 and 1.6 illustrate the basic topology for single and three phase PWM boost rectifiers.

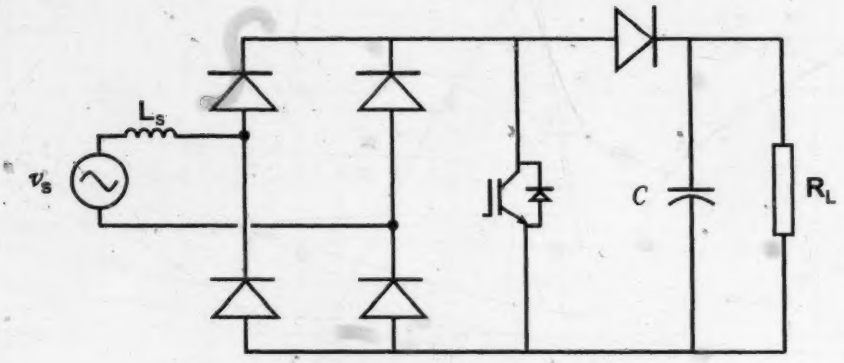


Figure 1.5: Single phase boost rectifier

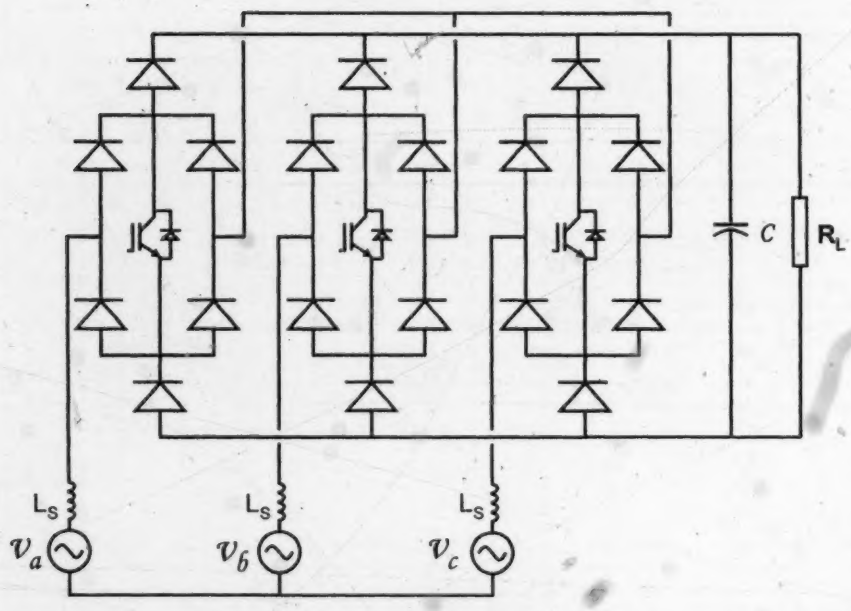


Figure 1.6: Three phase boost rectifier

Compared to bridge type PWM rectifiers, PWM boost rectifiers display key advantages such as:

- continuous input current with unidirectional power flow
- low complexity with only one active switch for single phase or three active switches for three phase configurations
- lower switching losses (three switching devices versus six for a bridge type topology)

- simple and robust control scheme; a control failure does not result in the short circuit of DC output voltage, thus guaranteeing high reliability

These advantages form the basis of wide applicability of PWM boost rectifiers in single and three phase industrial processes. This research work utilizes single and three phase PWM boost rectifier topologies for testing and verifying the operation of the proposed single and three phase current controllers (see Chapter 3).

1.3 Brief Introduction to Harmonic Distortions

Power system harmonics issues have existed since the early 1900s. The earliest discovered issues were third harmonic currents produced by saturated iron in machines and transformers. At the present, harmonic distortion constitutes one of the main concerns for engineers in several stages of energy utilization within the power industry. High levels of harmonic distortions can lead to problems for utility distribution systems, plant distributions systems, and any other exposed industrial instruments such as machines and transformers. Excessive presence of harmonics can lead to supply over-voltages and general heating of industrial instruments leading to eventual failure of the devices [1]. Today, there are many sources of harmonic distortions, making it increasingly necessary to address their influence on power systems.

Periodic waveforms are described mathematically as a series of sinusoidal waveforms summed together. Sinusoidal components are integer multiples of the fundamental frequency. Harmonics are integer multiples of fundamental frequency. Thus, the total harmonic distortion is the contribution of all harmonic frequency currents to the fundamental.

$$THD = \sqrt{\frac{sum\ of\ squares\ of\ amplitudes\ of\ all\ harmonics}{square\ of\ amplitudes\ of\ fundamental}} \times 100\% \qquad (1.2)$$

In this way, a summation of perfectly sinusoidal waveforms can give rise to a distorted waveform. Conversely, a distorted waveform can be represented as the superposition of the fundamental frequency waveform with other waveforms of different harmonic frequencies and amplitudes as indicated by figure 1.7.

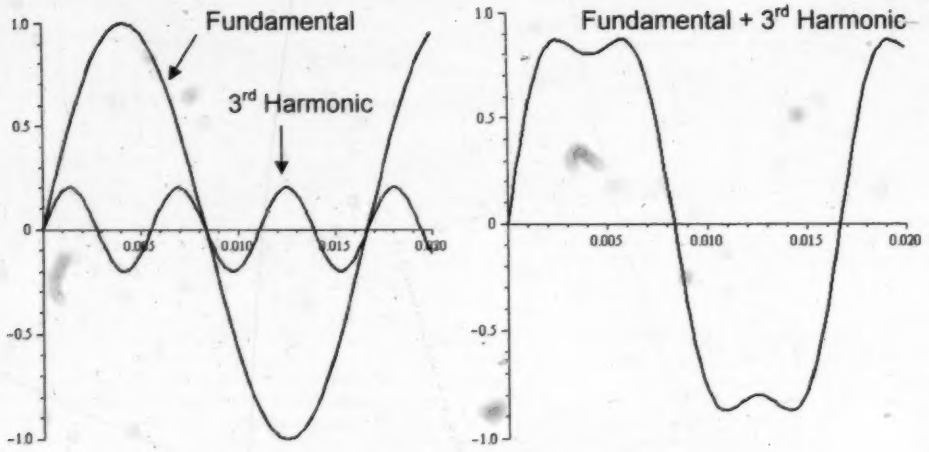


Figure 1.7: Distortion due to the 3rd harmonic

A better understanding of power system harmonic phenomena can be achieved with the consideration of two concepts: the nature of non-linear loads, and the interaction of harmonic currents and voltages within the power system. A linear load is one in which the current is proportional to the voltage. In general, the current waveform will have the same shape as the voltage waveform. A voltage and current waveform in a circuit with linear loads will show the two waveforms in phase with each other. Voltage and current involving inductors makes the voltage lead current; thus the two waveforms will be out of phase with each other. However, no waveform distortion will take place. Some examples of linear loads include incandescent lighting, electrical heaters, induction motors, current limiting reactors, induction generators, and power factor correction capacitor banks. Figure 1.8 illustrates the basic voltage and current waveforms for linear loads.

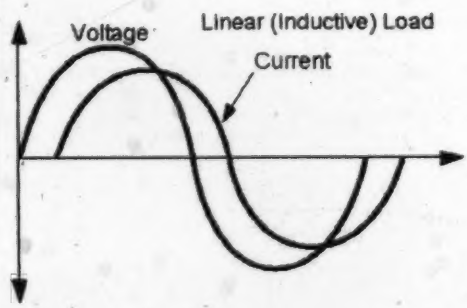


Figure 1.8: Basic voltage and current waveforms for linear loads

Conversely, non-linear loads are loads in which the current waveform does not resemble the applied voltage waveform. Among the most common nonlinear loads in industrial processes are power rectifiers. Some other examples of non-linear loads include variable frequency drives (VFD), DC motor controllers, cycloconverters, UPS, electric furnaces, and fluorescent lighting. Figure 1.9 illustrates the basic voltage and current waveforms for a typical non-linear load.

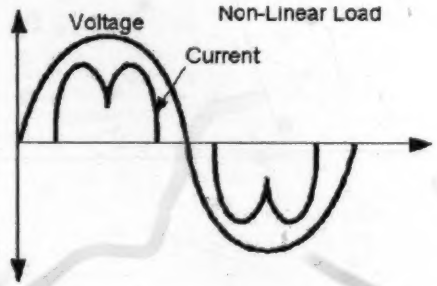


Figure 1.9: Basic voltage and current waveforms for non-linear loads

High levels of harmonic distortion can lead to problems for the utility distribution system by reducing its overall efficiency. A power system has a natural resonant frequency which is determined by the inductance and capacitance of the system. This resonant frequency coinciding with a characteristic harmonic present at the site can produce a large overvoltage, resulting in excessive equipment heating and even failure of vital components. In transformers for example, winding losses increase due to higher frequency current components. This can cause additional heating of the transformer windings leading to inefficiency and even winding failure in extreme cases. Similarly, harmonic voltages and currents have similar impact on motors as voltage phase imbalance. The presences of higher frequency current components cause additional rotor heating, which significantly shortens motor life.

A common solution for reducing harmonic distortion is through the connection of passive filters, which are tuned to filter out a specific harmonic frequency. A typical configuration of a single phase passive filter is shown in figure 1.10.

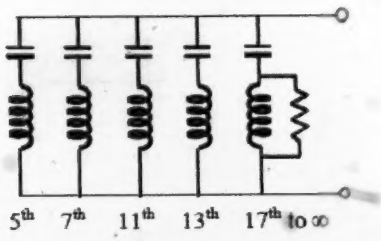


Figure 1.10: Passive harmonic filter for single phase applications

Passive filters are generally regarded as unsuitable for filtering 3rd harmonics. Thus, they are well suited for applications where 3rd harmonics are generally not an issue. In contrast to passive filters, active harmonic filters monitor the supply current and inject a harmonic current of equal magnitude but opposite polarity to dynamically cancel the harmonic currents. This task is typically accomplished via the use of various current control techniques.

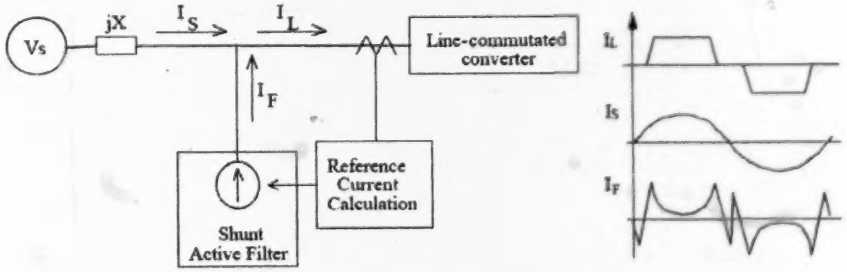


Figure 1.11: Active harmonic filter for single phase application

In addition to the above solutions for harmonic mitigation, PWM rectifiers employing current control are also highly effective in reducing the harmonic content in the supply currents while providing a unity input power factor.

1.4 Thesis Summary

This thesis work is focused on the design and implementation of novel PWM current control techniques for single and three phase boost rectifier topologies which are capable of providing UFPF operation with low input current THD. Comparisons between the proposed current control techniques and the proportional-integral (PI)

current control schemes for single and three phase utility rectifiers are presented. The proposed current control techniques utilize the advantages of both hysteresis current control and carrier based current control schemes (see Chapter 3).

The behaviour of the proposed current control scheme is analyzed under both single phase and three phase operating conditions. An investigation through comprehensive single and three phase simulations indicates the advantages of the proposed scheme over the PI control scheme, such as stable steady-state operation, quick transient responses with minimal overshoots and an inherent tolerance to system disturbances such as DC offsets (see Chapter 4). Analog realizations of the current controllers are developed and implemented based on theoretical and simulation results (see Chapter 5). The experimental results demonstrate excellent performance of the controllers and present good agreement between the simulations and experiments (see Chapter 6).

1.5 Summary

Harmonic saturated power utilities are a major source of problems in today's industry. Single and three phase uncontrolled rectifiers are the most widespread source of harmonic distortions in the utility systems. PWM rectifiers have the advantages over uncontrolled rectifiers of providing sinusoidal supply and a unity fundamental power factor; thus reducing the total harmonic distortion in the system. This thesis is focused on the design and implementation of PWM current control techniques for single and three phase boost rectifier topologies. The proposed control schemes are capable of providing sinusoidal input currents and a unity fundamental power factor. The current control schemes are designed for low complexity and high overall performance at a low implementation cost.

Chapter 2 PWM Current Control Techniques

The performance of a converter system is highly dependant on the current control scheme being utilized. In the past few decades, significant work has been conducted on adequate current control schemes for PWM rectifiers to ensure the highest power quality. In general, a current control strategy must provide ideal tracking by allowing no phase or amplitude errors, fast transient response to provide high system dynamics, and a constant switching frequency to ensure safe operation of semiconductor devices. Furthermore, low harmonic content is also used as one of the requirements for a current control scheme. This chapter introduces some of the most common current control techniques used in the industry.

Compared to conventional open-loop voltage controlled PWM rectifiers, current controlled PWM rectifiers have the following advantages [2]:

- Accurate control of instantaneous input current waveform resulting in low harmonic content
- Unity fundamental power factor
- Peak current protection
- Fast transient response leading to high system dynamics
- Compensation of effects due to load parameter variations and semiconductor voltage drops
- Compensation of the DC link and utility voltage variations
- Regenerative capability which allows control of bidirectional power flow

Existing current control strategies can achieve low harmonic distortions while maintaining a unity fundamental power factor. The overall cost and complexity of the scheme is highly dependant on the quality of the control required. Research is still underway to improve upon current control techniques; however, several current control techniques have been successfully implemented. A few examples of prevalent single and three phase current control techniques are subsequently summarized and are used to place the proposed current control techniques in context to the previously studied work.

2.1 Linear Current Control Techniques

In general, linear current controllers have clearly separated current error regulation and voltage modulation parts. As such, linear control schemes commonly utilize open-loop voltage modulators such as SPWM and space-vector modulators. Voltage-type PWM modulators have the inherent advantage of providing a fixed switching frequency with a well defined harmonic spectrum. Furthermore, linear controllers have the advantage of being more robust to system parameter variations as compared to non-linear control techniques. The following linear current control schemes are most commonly used in industrial applications: stationary reference frame current control using PI compensators, synchronous vector control, predictive and deadbeat current control.

2.1.1 Stationary Frame Current Controller Using PI Compensators

Current controllers using PI compensators in the stationary reference frame are the most commonly employed current control schemes in single and three phase applications. This scheme is used as a comparison basis for the proposed current control schemes. The stationary current controller utilizes proportional-integral (PI) compensators to minimize the error between the measured currents and its reference value within a fixed frequency band. Either one PI compensator or three separate PI compensators are used depending on whether the application is single or three phase in nature; however, the general control concept is the same regardless of the single or three phase nature of the current controller. Figure 2.1 illustrates the basic block diagram of a three phase stationary reference frame current controller utilizing PI compensators.

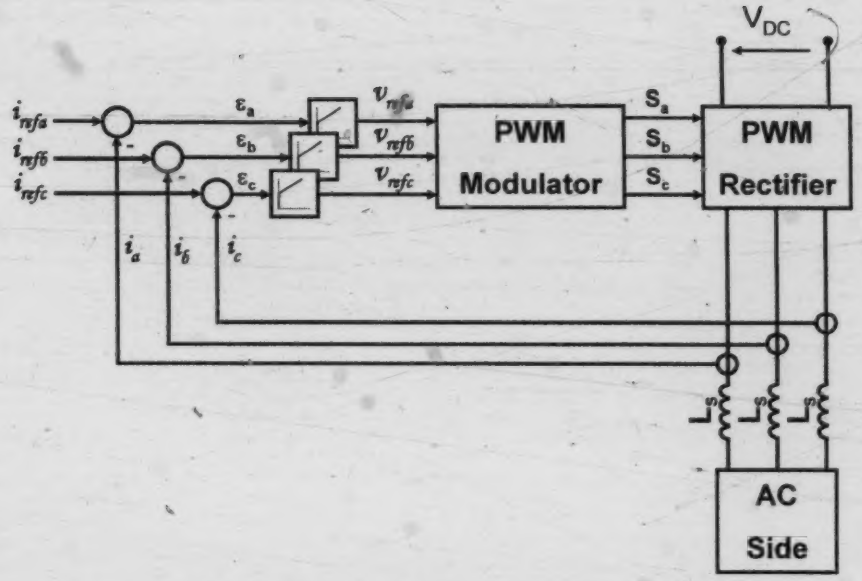


Figure 2.1: Stationary frame current control using PI compensators

In essence, the error signal is obtained by taking a difference between the reference signal and its respective measured current. The instantaneous current error is fed to the PI compensator, which produces the sinusoidal voltage reference signal (i.e. the sinusoidal modulation reference signal for PWM). The integral term in the PI compensator improves the tracking by reducing the instantaneous current error at low frequency between the reference and the actual current while the proportional gain affects the overall current ripple. This voltage reference signal is compared with a triangular carrier signal. If intersections are obtained, the voltage reference signal is forced to remain within the band defined by the amplitude of the triangle wave carrier; thus generating the PWM switching signal. In this scheme, the switching time of the semiconductor devices is influenced due to the feedback of the input current ripple. In stationary PI current control, the slope of the sinusoidal voltage reference signals must never exceed the slope of the triangle wave carrier since this can result in the generation of improper switching patterns leading to control instability.

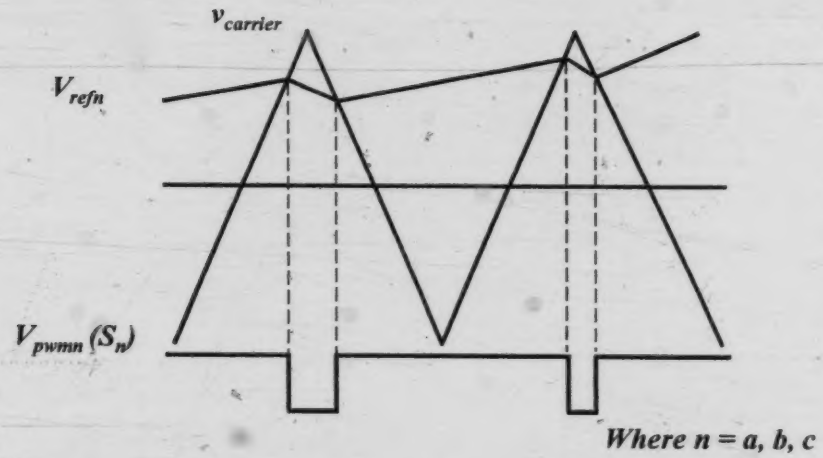


Figure 2.2: Generation of PWM in stationary PI current control

Stationary PI current controllers offer a simple and inexpensive control strategy; however, this technique has inherent amplitude and phase tracking errors which are caused by unbalanced supply conditions and consequently result in inaccurate control of the PWM rectifier. However, amplitude and phase tracking errors can be compensated by using phase locked-loop (PLL) circuits or feed forward correction [2]. This work is focused on how to overcome the tracking error in the current signal by combining the functionality of hysteresis current control techniques with carrier based controllers.

2.1.2 Synchronous Vector Current Controller

Some industrial processes are highly sensitive. Slight phase or amplitude errors can lead to improper system operation. As a result, synchronous current controllers have become a standard solution for most industrial applications. Unlike stationary reference control schemes, synchronous vector controllers are almost exclusively used in three phase applications. Synchronous vector controllers are based on the space vector approach. The space vector approach uses field orientation (Clarke-Park transformation) to convert three phase current vectors from a stationary reference frame to a two dimensional rotating d-q frame. In general, a rotating transformation which transforms the phase variables (abc) to a rotating axis on the d-q plane can be expressed as:

$$\begin{bmatrix} f_q \\ f_d \\ f_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \quad (2.1)$$

The angle θ is the angular displacement of the vector on the d-q plane measured with respect to the projection of the "a" axis onto this plane. It should be noticed that the zero axis does not enter into the rotational transformation and hence, the zero axis can be considered as the axis about which the rotation takes place (i.e. axis of rotation) [9]. Due to this coordinate transformation, the f_q *and* f_d are DC components. Figure 2.3 illustrates a block diagram of a synchronous vector controller in a rotating d-q reference frame.

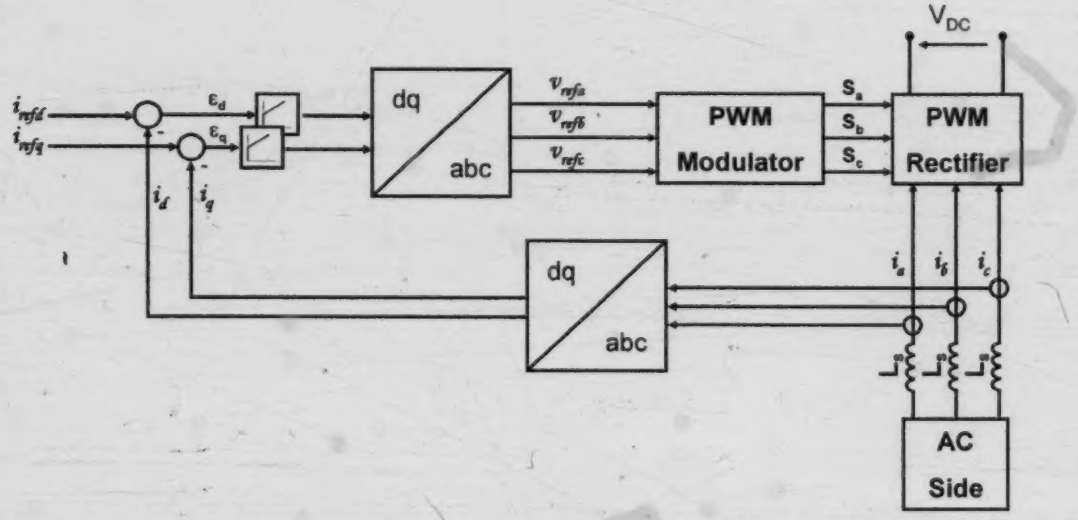


Figure 2.3: Synchronous vector controller in rotating reference frame

The synchronous vector controller in figure 2.3 utilizes two PI compensators to force the instantaneous current error to zero. The output of the PI compensators are then converted back into the three dimensional stationary reference frame in order to obtain the three sinusoidal voltage reference signals necessary for PWM generation. In the synchronous reference frame, the d-axis represents the reactive power whereas the q-axis represents real power. Thus, in order to achieve UFPF operation with synchronous

vector controller, it is necessary to ensure that the reference signal for the d-axis current is equal to zero (i.e. $i_{refd} = 0$).

As a result of redundancy in the three phase variable representation (abc), it is possible to transform the system to an equivalent two phase representation (αβ). Alternatively, it is possible to perform current vector control in a stationary reference frame [9]. In this control scheme, Clarke's transformation is used to convert three phase vectors from a stationary reference frame to a two dimensional stationary reference frame (αβ). This transformation from three phase to two phase quantities can be expressed in the following matrix form.

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & \cos(\gamma) & \cos(2\gamma) \\ 0 & \sin(\gamma) & \sin(2\gamma) \end{bmatrix}\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \qquad where \quad \gamma = \frac{2\pi}{3} \tag{2.2}$$

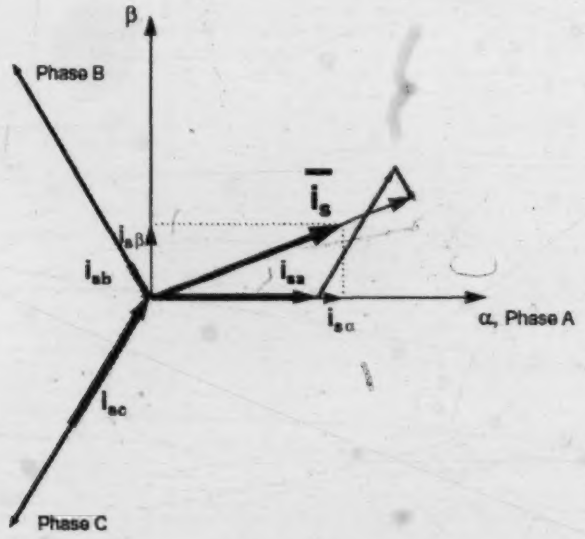


Figure 2.4: Current space vector projection

This method utilizes a variable frequency generator to generate the voltage reference signals $v_{\alpha ref}$ and $v_{\beta ref}$. These voltage reference signals are then converted back to the three dimensional stationary reference frame in order to obtain the sinusoidal voltage reference signals necessary for three phase PWM.

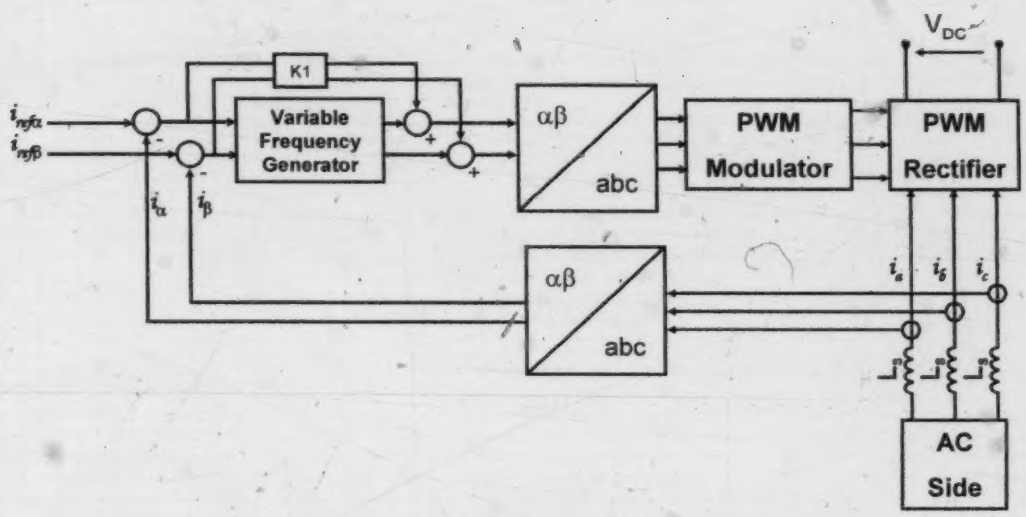


Figure 2.5: Synchronous vector control in stationary reference frame

2.1.3 Predictive and Deadbeat Control

Predictive current control predicts the current error vector by sampling the actual currents at the beginning of each sampling period and comparing them to the reference current vectors. The voltage space vector, which reduces the current error vector to zero, is then computed using a model of the supply (or load) parameters.

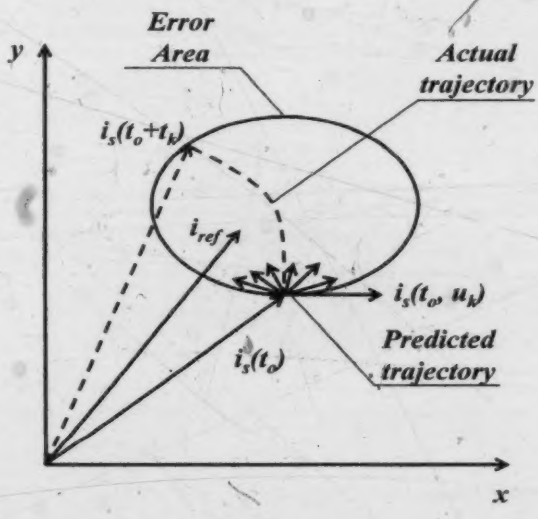


Figure 2.6: Error curve in predictive current control algorithm [2]

The location of the error curve in the predictive current controller algorithm is determined by the reference current vector. When the actual current vector approaches a point on the error curve, seven different trajectories of the current are predicted, one for each possible (six active and zero) converter voltage vectors [10]. The algorithm then utilizes an optimization procedure based on the supply (or load) parameters to calculate the voltage vector which minimizes the current error vector to zero.

Deadbeat current controllers are simply predictive controllers where the voltage space vector is chosen to force the current error vector to zero at the end of the sampling period. In a conventional implementation, predictive controllers calculate the voltage space vector so as to make the actual phase currents reach their respective reference currents by the end of the sampling period. These calculations are often performed in the two dimensional stationary reference frame ($\alpha\beta$). However, it should be noted that the shape of the error curve is independent of the choice of particular coordinates and, therefore, the predictive current controller can be implemented in any rotating or stationary reference coordinates [2, 6, 7, 10]. Deadbeat controllers do not require the measurement of the voltage space vector. The algorithm of the controller provides a voltage space vector necessary to force the current error vector to zero. Figure 2.7 illustrates a basic block diagram of a three phase deadbeat current controller.

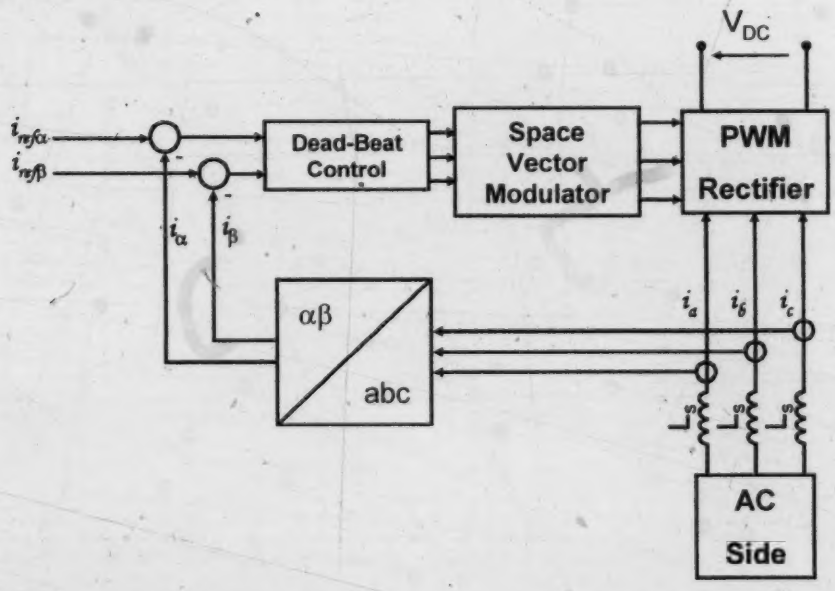


Figure 2.7: Basic scheme of a deadbeat current controller

Predictive and deadbeat controllers are capable of providing high system dynamics with little tracking error; however, these control methods have a dependency on microprocessors for vector computations which adds to the complexity and cost of the current controller. Due to the nature of their design, predictive and deadbeat controllers are highly sensitive to variations in system parameters.

2.2 Non-linear Current Control Techniques

In general, the use of PWM modulators in linear controls provides a well defined harmonic spectrum, but their dynamic properties are inferior to those of non-linear controls. Common non-linear current control techniques include hysteresis band current control as well as intelligent control schemes such as fuzzy logic current control.

2.2.1 Hysteresis Band Current Control

Hysteresis control schemes are based on a non-linear feedback loop with hysteresis comparators which compare the measured current with a reference signal representing the desired current value. The switching signals for the PWM converter are directly developed by the hysteresis comparators whenever the current error exceeds an assigned tolerance band. It is characteristic for the hysteresis current controllers that the instantaneous current is kept in a tolerance band (See figure 2.8).

In general, hysteresis current controllers are simple; however, these controllers can become considerably complex depending on the application. Hysteresis current controllers exhibit little or no tracking errors while maintaining high system dynamics. However, for hysteresis current controllers, switching frequency is highly dependant on system parameters and can vary with the supply voltage. As a result, this control scheme is sensitive to system parameters and supply voltage imbalances.

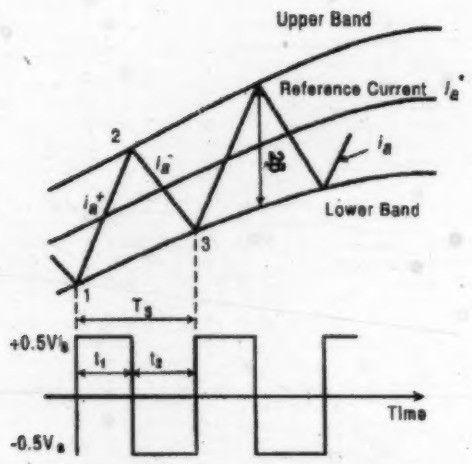


Figure 2.8: Basic hysteresis concept

Various proposals have been put forward on how to overcome this varying frequency. The most common approach involves the use of an adaptive hysteresis technique which varies the tolerance band amplitude according to the supply voltage. Among the several adaptive hysteresis schemes, significant works in the development of adaptive hysteresis current control are presented next. Bose [11] utilized a DSP-based adaptive hysteresis control scheme in which the hysteresis band is modulated as a function of system parameters to provide a near constant switching frequency while providing stable control and fast system dynamics. More recently, Yao and Holmes [12] presented a simple scheme for varying the hysteresis band by using both feed-forward and feedback control strategies to achieve constant switching frequency without requiring a precise knowledge of the system parameters. Alternatively, several researchers have experimented with the use of PLL control to lock the switching frequency to a single value [2, 10].

Although adaptive hysteresis control schemes are more complex in nature than schemes with a fixed hysteresis band, they guarantee very fast response together with little or no tracking error. As a result, adaptive hysteresis controllers are well suited for high performance high speed applications.

2.2.2 Fuzzy Logic Control Schemes

There has been tremendous growth in the use of fuzzy logic controllers in power systems as well as power electronic applications. Fuzzy logic controllers utilize descriptive rules and as a result a mathematical model of the power converter is not needed. This improves the robustness of the control to system nonlinearities and parameter variations. Controllers based on fuzzy logic overcome most of the shortcomings of the most commonly used linear and non-linear control schemes.

In basic current control applications, the fuzzy logic controller is used as a substitute for the conventional PI compensator [13, 14]. The current error between the measured current and its respective reference signal provides the fuzzy logic controller input crisp values. The controller then processes this error through a series of membership functions called fuzzification, similar to conventional proportional and PI compensators. The fuzzified output is evaluated according to control rules and then defuzzified to produce the crisp output commands (i.e. the voltage reference signals for PWM modulator).

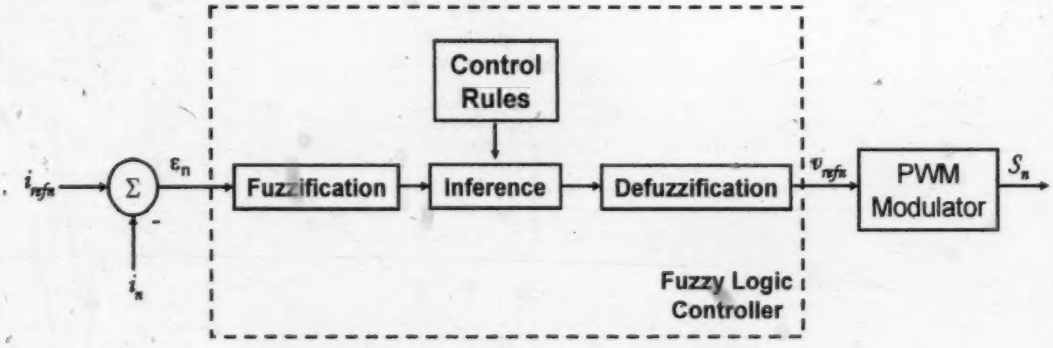


Figure 2.9: Basic fuzzy logic current control scheme

The choice of the membership functions and fuzzy logic control rules depends on prior knowledge of the system. The use of fuzzy logic controllers in current control applications can significantly reduce tracking error and transient overshoots [13, 14, 15]. The main advantages of fuzzy logic controllers are that they do not require extensive mathematical model of the process, are adaptive, simple to implement, and relatively immune to noise and system parameter variations [2, 9, 10]. However, even though the general design rules for designing fuzzy logic controllers are known, fine tuning of the

control is done heuristically and requires time. Thus, the design procedure and resulting performance of the fuzzy logic controller is highly dependant on the knowledge and experience of the designer.

2.3 Summary

Current control techniques have garnered intensive interest of researchers due to the wide spread applications of PWM rectifiers in single and three phase industrial applications. A brief review of prevalent linear and non-linear current control techniques applicable to single and three phase PWM rectifiers was provided. The basic principles of these current control techniques as well as their advantages and disadvantages were described. This work combines the advantages of hysteresis based current controllers with those of carrier based control schemes to achieve a constant switching frequency and zero current tracking error while maintaining stable control with fast transients and high system dynamics. The proposed single and three phase current control schemes maintain low complexity; thus allowing for easy and cost effective implementation with readily available analog components.

Chapter 3 Hybrid Current Control Using Hysteresis and Carrier Based Control Schemes

In the past, literature has always treated hysteresis controllers and fixed frequency carrier based control schemes separately as independent current control schemes. More recently, hybrid current controllers, which can be regarded as an integration of the above two, have been extensively investigated [8, 18-20]. These controllers combine the excellent current wave shaping ability of hysteresis based controllers together with the constant switching frequency of carrier based controllers; resulting in a control scheme which is highly insensitive to variations in system parameters. The proposed current control schemes are based on hybrid current control techniques and thus maintain advantages inherent to both hysteresis and carrier based controllers.

Theoretical analysis of the proposed current control schemes is presented in this chapter. A relationship between the modulation depth signal (fundamental voltage at the rectifier input terminals necessary to draw sinusoidal current) and the average of the PWM output signal is presented. The methods to obtain suitable modulation depth signal are investigated for single and three phase applications. Furthermore, the control of the peak-to-peak amplitude of the current error signal is studied so as to provide a zero average current error. The subsequent chapters of this thesis are focused on the development of the proposed hybrid current control techniques for single and three phase PWM boost rectifiers.

3.1 Hysteresis Comparator

The relationship between modulation depth signal (m_a) and the average of the PWM signal is presented by analyzing a hysteresis comparator under unipolar PWM operation. Figure 3.1 illustrates a self-oscillating closed-loop system where the unipolar PWM output of the hysteresis comparator is fed back into an integrator.

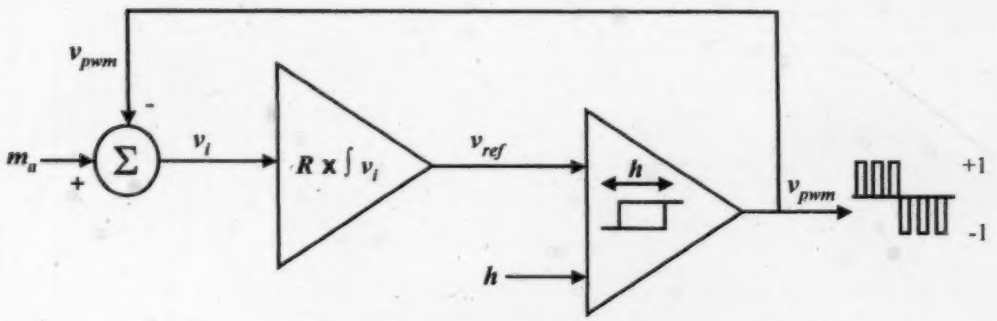


Figure 3.1: Hysteresis PWM signal comparator

The slope of v_{ref} is determined by the integration constant R, the modulation depth signal m_a, and the unipolar PWM signal. The peak-to-peak ripple of v_{ref} is bounded by the upper and lower limits of the hysteresis band (h) and the direction of its slope depends upon the polarity of the PWM signal. Understanding the operation of the self oscillating closed-loop system in figure 3.1 is crucial for determining the relationship between the modulation depth signal and the average of the PWM waveform. Figure 3.2 shows expanded waveforms of a delta-modulated hysteresis PWM controller.

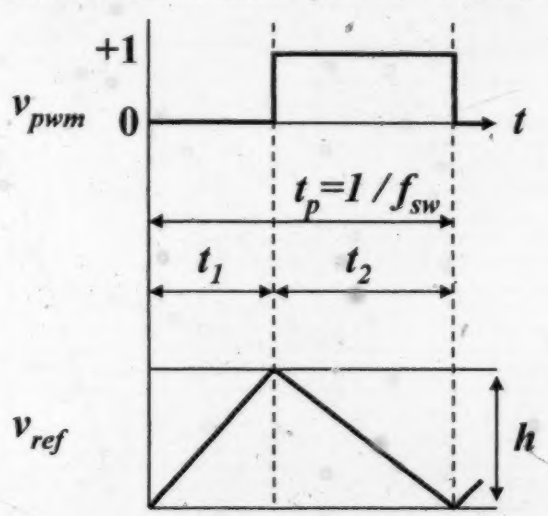


Figure 3.2: Ramping rate of v_{ref}

Assuming a dimensionless system where the amplitude of m_a ranges between ±1 and the PWM signal has states 0 and +1 in the positive half cycle, the ramping rate of v_{ref} for a positive m_a is given by:

$$t_1 : \frac{dv_{ref}}{dt}(t_1) = R \times m_a, \qquad t_2 : \frac{dv_{ref}}{dt}(t_1) = R \times (m_a - 1) \tag{3.1}$$

Hence, the periods t_1 and t_2 are obtained by taking the ratio of the hysteresis band over the ramping rate of v_{ref}.

$$t_1 = \frac{h}{R \times m_a}, \qquad t_2 = \frac{h}{-R \times (m_a - 1)} = \frac{h}{R \times (1 - m_a)} \tag{3.2}$$

Thus, the total period and the resultant switching frequency of the PWM waveform are given by:

$$t_p = t_1 + t_2 = \frac{h}{R \times m_a (1 - m_a)} \tag{3.3}$$

$$f_{sw} = \frac{1}{t_p} = \frac{R}{h} \times m_a (1 - m_a) \tag{3.4}$$

It is worthwhile noting that the PWM switching frequency is dependant on the ratio of the integration constant and the hysteresis band as well as on the modulation depth signal. Having more than one dependency for the switching frequency is undesirable in PWM current control applications. In order to determine the relationship between the average of the PWM signal and the modulation depth signal, the ratio of on-time over the total period of the PWM signal needs to be analyzed (i.e. the duty cycle of the PWM pulses).

$$v_{pwm,ave} = \frac{t_2}{t_p} = \frac{\frac{h}{R} \times \frac{1}{(1 - m_a)}}{\frac{h}{R} \times \frac{1}{m_a (1 - m_a)}} = m_a \tag{3.5}$$

Equation (3.5) states that for any arbitrary hysteresis band and integration constant, the average of the PWM signal is equal to the magnitude of the modulation depth signal.

3.2 PWM Comparator Using Carrier Signal

Figure 3.3 illustrates a self oscillating closed-loop system much like the one discussed in section 3.1; however, instead of using a hysteresis band, this system utilizes two triangle wave carriers to generate a unipolar PWM signal at a fixed frequency.

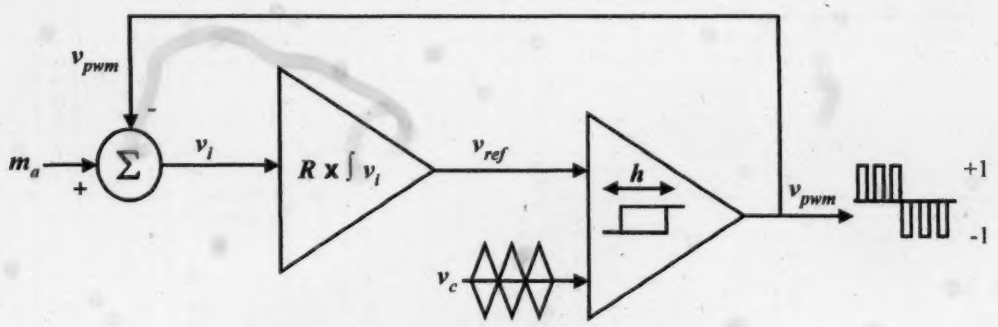


Figure 3.3: PWM comparator using carrier signal

Given a carrier frequency f_c, the frequency and period of the resultant unipolar PWM signal are given by:

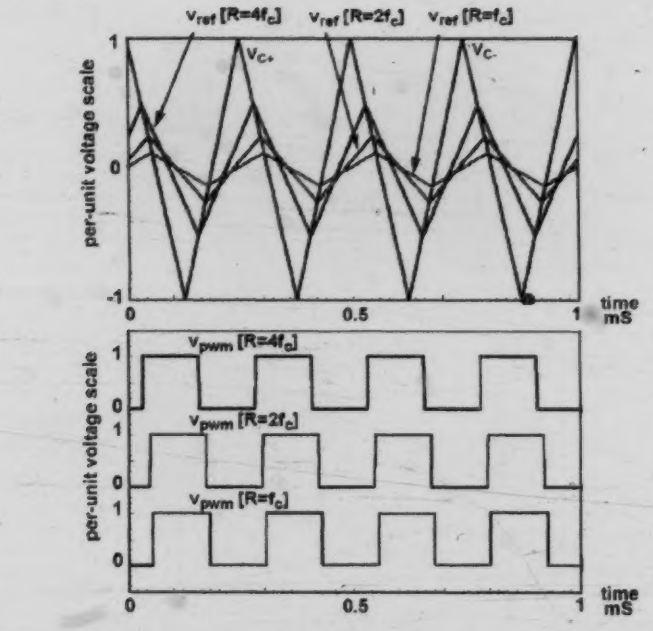
$$f_{sw} = 2f_c \tag{3.6}$$

$$t_p = \frac{1}{f_{sw}} = \frac{1}{2f_c} \tag{3.7}$$

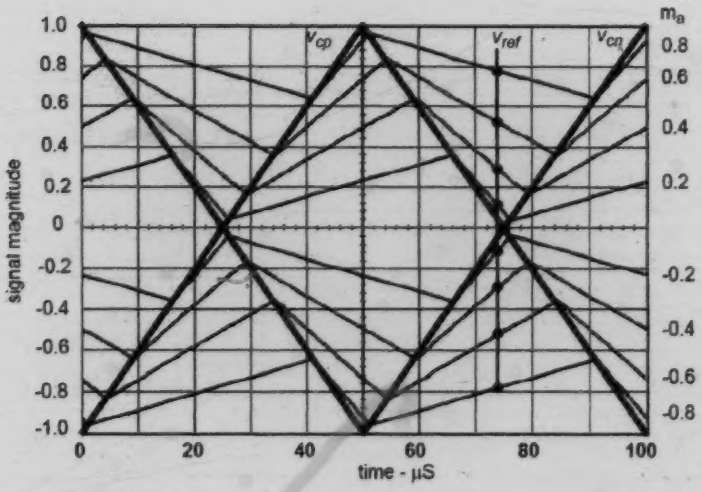
The variation of the peak-to-peak amplitude of v_{ref} over a PWM cycle depends on the magnitude of the modulation depth signal; however, this peak-to-peak ripple is bound between an upper and a lower limit. Thus it is suitable to assume that the peak-to-peak variation of the v_{ref} signal (Δv_{ref}) is equivalent to the hysteresis band from the previous subsection. Thus using equation (3.4), the peak-to-peak amplitude of v_{ref} is given by:

$$\Delta v_{ref} = \frac{R}{f_{sw}} \times m_a(1 - m_a) = \frac{R}{2f_c} \times m_a(1 - m_a) \tag{3.8}$$

From equation (3.8), it is apparent that the maximum peak-to-peak ripple for v_{ref} occurs when $m_a = 0.5$. for an arbitrary integration constant. Furthermore, equation (3.8) states that Δv_{ref} is dependant on two variables: the integration constant R, which varies with system parameters such as supply inductance, and the modulation depth signal m_a, which is a varying sinusoidal signal. The dependency on a variable which varies due to system parameters is an undesirable trait for PWM current control applications.



(a)



(b)

Figure 3.4: v_{ref} and PWM waveforms for m_a = 0.5 at f_c = 5kHz

Figure 3.4 illustrates the effects of integration constant on the PWM signal. The varying integration constant introduces a negligible phase shift in the PWM signal relative to the carrier signal. As a result, the integration constant can be allowed to vary

over a wide range and does not need to be necessarily constant in order to obtain accurate control of the PWM signal. The ability of controller to cope with and overcome system variations is highly desirable in practice. Thus, it can be safely assumed that the average of the PWM signal in this closed-loop system is approximately equivalent to the magnitude of the modulation depth signal.

3.3 The Proposed Single Phase Current Control Technique

Figure 3.5 illustrates a general block diagram of the proposed single phase current control scheme.

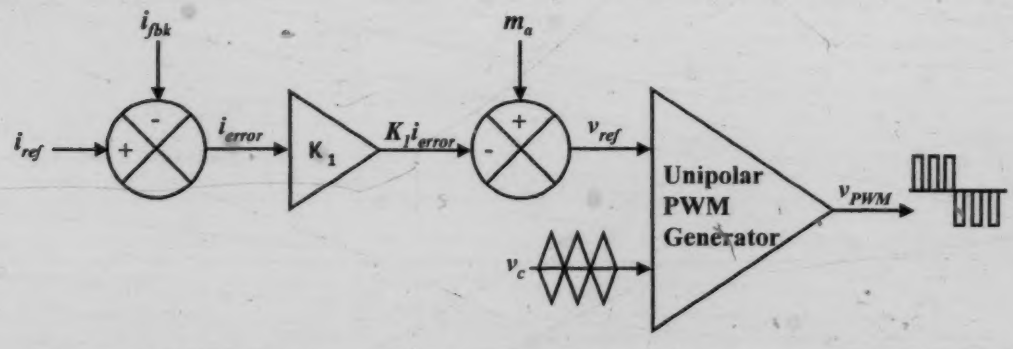


Figure 3.5: Basic block diagram of the proposed single phase current control scheme

In its most basic form, the proposed control scheme in figure 3.5 uses the difference between the modulation depth signal and the current error signal to generate the sinusoidal voltage reference ($v_{ref} = m_a - K_1 i_{error}$) for PWM signal generation. Assuming unity power factor operation, m_a represents the fundamental voltage at the rectifier input terminals required to draw the desired in phase sinusoidal current from the AC supply; however, the ideal modulation depth signal required to force the current error to zero is difficult to produce. The successful implementation of the proposed control scheme relies on the upon the appropriate choice of K_1, which limits the peak-to-peak amplitude of the high frequency ripple in the current error signal, as well as the ability to generate an m_a which closely resembles the required ideal modulation depth signal [8].

3.4 The Proposed Three Phase Current Control Technique (3-Current Controller)

Figure 3.6 illustrates a general block diagram of the proposed three phase current control scheme.

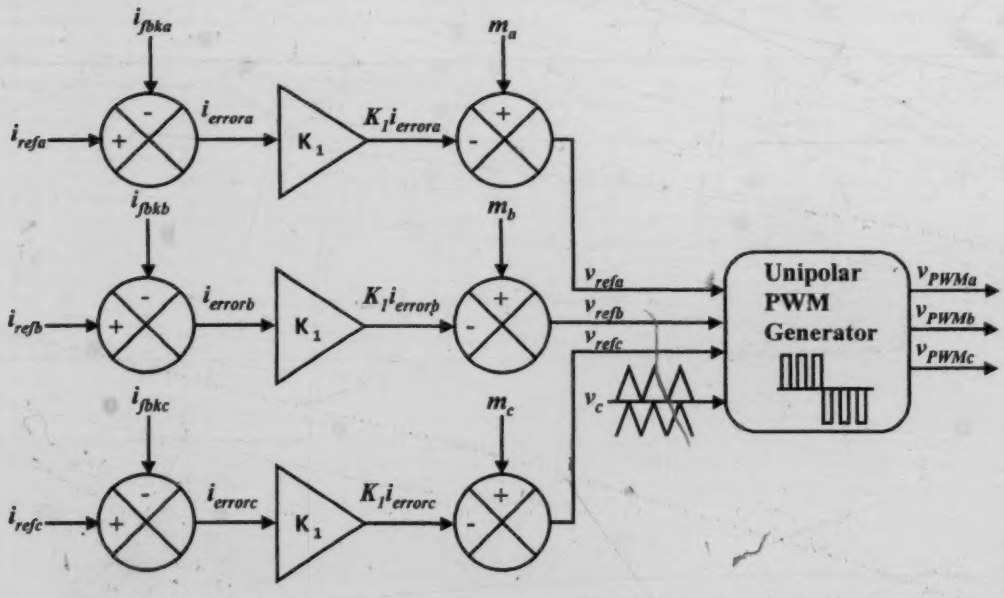


Figure 3.6: Block diagram of the proposed three phase current control scheme

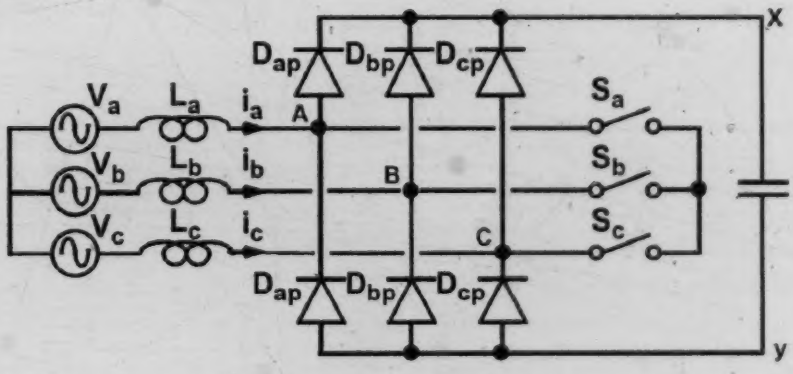
Similar to the proposed single phase current control technique, the three phase current controller uses the subtraction of the current error signals from their respective modulation depth signals to generate the voltage references (v_{refa}, v_{refb}, v_{refc}) necessary for generating the PWM signals. Although the three phase currents are coupled (i.e. each phase current not only depends on the corresponding phase voltage but is also affected by the voltage of the other phases due to interference between the commutations of the three phases), it is possible to design each controller independently. Thus, the design of the controller is simplified when considering each phase separately. This allows for the implementation of the proposed single phase current controller in three phase applications (i.e. the single phase controller is implemented independently for each phase).

Three phase current control schemes are prone to the effects of interference between phases due to phase coupling; however, the proposed three phase current control

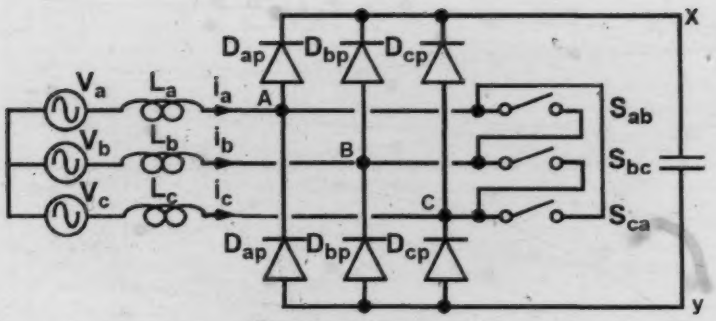
scheme minimizes the interaction between the three phases by using the feedback of the modulation depth signals. Similar to the single phase controller, the three phase modulation depth signals (m_a, m_b, m_c) represent the fundamental of the respective phase voltages at the rectifier input terminals required to draw the desired in phase sinusoidal phase currents (i_a, i_b, i_c) from the three phase supply. Similarly, successful implementation of the controller depends on the appropriate choice of the K_1 gain factor and the ability to generate the modulation depth signals which closely resemble their ideal cases.

3.5 Proposed 2 - Current Control Technique (or Dual Current Control Mode)

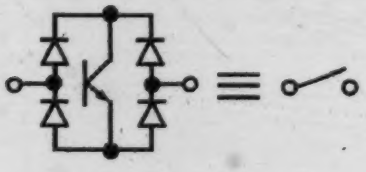
The control of three line-currents involves the use of three independent controllers which simultaneously control the three phase currents. The proposed three phase current controller discussed in section 3.4 deals with the operation of a three phase PWM boost rectifier with star (wye) connected switches; the 2-current control technique allows the controller to be implemented on both star connected and delta connected switches. In the dual current control mode, only two switches are being switched at any given instance while the third switch is either on (star), or off (delta). As a result, at any given time, only two currents are being controlled in the dual current control mode; resulting in lower switching losses. This section examines the 2-current control technique for both the star-connected and delta-connected three phase bidirectional switch PWM boost rectifiers (see figure 3.7 (a)-(b)).



(a) Star-connected bidirectional switch boost rectifier



(b) Delta-connected bidirectional switch boost rectifier



(c) Bidirectional switch

Figure 3.7: Three phase boost rectifier circuit topologies

The rectifier topologies in figure 3.7 (a)-(b) can be made to operate over a 60° as though they consisted only of the components in the general sub-topology model illustrated in figure 3.8. The current controller interprets which line currents and rectifier devices correspond to the sub-topology elements.

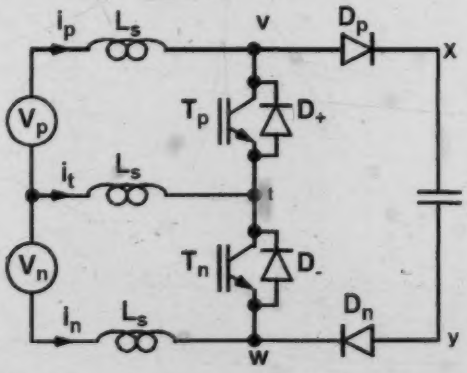


Figure 3.8: General sub-topology model for star-connected and delta-connected switch boost rectifier

The signals v_p and v_n form a dual stacked dc input voltage. The two input voltages can be expressed by the following equations:

$$v_p = p - t \tag{3.9}$$

$$v_n = n + t \tag{3.10}$$

The shape of the voltage waveform p corresponds to the profile of the most positive phase voltage and n corresponds to the most negative phase voltage (see figure 3.9).

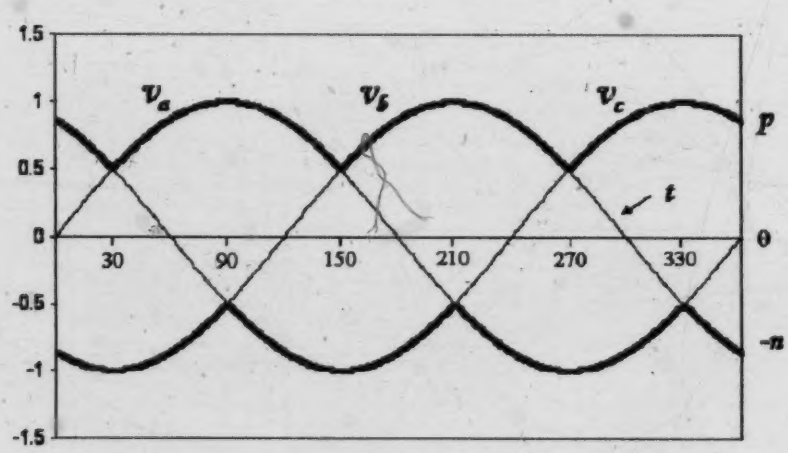


Figure 3.9: Sub-topology control signals p, n, and t

Using the phase definition in figure 3.9, Table I shows how various parameters in the sub-topology can be related to the actual rectifier topology for each 60° period.

Table 3-I: Sub-Topology Configuration Over 360°

60° Periods	Sub-topology circuit parameters							
	v	t	w	v_p	v_n	i_p	i_t	i_n
330°-30°	C	A	B	V_{ca}	V_{ab}	i_c	i_a	i_b
30°-90°	A	C	B	V_{ac}	V_{cb}	i_a	i_c	i_b
90°-150°	A	B	C	V_{ab}	V_{bc}	i_a	i_b	i_c
150°-210°	B	A	C	V_{ba}	V_{ac}	i_b	i_a	i_c
210°-270°	B	C	A	V_{bc}	V_{ca}	i_b	i_c	i_a
270°-330°	C	B	A	V_{cb}	V_{ba}	i_c	i_b	i_a

Table II relates the actual circuit components in the star and delta configurations to the sub-topology components for each 60° period.

Table 3-II: Sub-Topology Components

60° Periods	Star			Delta			Star and Delta			
	T_p	S_{on}	T_n	T_p	S_{off}	T_n	D_+	D_-	D_p	D_n
330°-30°	S_c	S_a	S_b	S_{ca}	S_{bc}	S_{ab}	D_{ap}	D_{an}	D_{cp}	D_{bn}
30°-90°	S_a	S_c	S_b	S_{ca}	S_{ab}	S_{bc}	D_{cp}	D_{cn}	D_{ap}	D_{bn}
90°-150°	S_a	S_b	S_c	S_{ab}	S_{ca}	S_{bc}	D_{bp}	D_{bn}	D_{ap}	D_{cn}
150°-210°	S_b	S_a	S_c	S_{ab}	S_{bc}	S_{ca}	D_{ap}	D_{an}	D_{bp}	D_{cn}
210°-270°	S_b	S_c	S_a	S_{bc}	S_{ab}	S_{ca}	D_{cp}	D_{cn}	D_{bp}	D_{an}
270°-330°	S_c	S_b	S_a	S_{bc}	S_{ca}	S_{ab}	D_{bp}	D_{bn}	D_{cp}	D_{an}

Assuming i_p and i_n are shaped such that they follow v_p and v_n as a reference, then i_t takes the wave-shape of the voltage signal t shown in figure 3.9. The currents i_p and i_n can be controlled by operating sub-topology as a stacked dual boost rectifier. For example, i_p can be increased by turning on switch T_P and decreased by turning off T_P. The actual device switching pattern for the star-connected and delta-connected bidirectional switch PWM boost rectifiers can be obtained directly from Table II. Tables III and IV illustrate how three phase PWM switching signals for the rectifier input current are directed to the actual rectifier switches in order to implement the 2-current control technique for the specified sub-topology.

Table 3-III: Switching Pattern for Star-Connected PWM Boost Rectifier

60° Periods	Star		
	S_a	S_b	S_c
330°-30°	ON	$\overline{\text{PWMb}}$	PWMc
30°-90°	PWMa	$\overline{\text{PWMb}}$	ON
90°-150°	PWMa	ON	$\overline{\text{PWMc}}$
150°-210°	ON	PWMb	$\overline{\text{PWMc}}$
210°-270°	$\overline{\text{PWMa}}$	PWMb	ON
270°-330°	$\overline{\text{PWMa}}$	ON	PWMc

Table 3-IV: Switching Pattern for Delta-Connected PWM Boost Rectifier

60° Periods	Delta		
	S_{ab}	S_{bc}	S_{ca}
330°-30°	$\overline{\text{PWMb}}$	OFF	PWMc
30°-90°	OFF	$\overline{\text{PWMb}}$	PWMa
90°-150°	PWMa	$\overline{\text{PWMc}}$	OFF
150°-210°	PWMb	OFF	$\overline{\text{PWMc}}$
210°-270°	OFF	PWMb	$\overline{\text{PWMa}}$
270°-330°	$\overline{\text{PWMa}}$	PWMc	OFF

Figure 3.10 shows the proposed three phase current control scheme extended to operate under the dual current control mode.

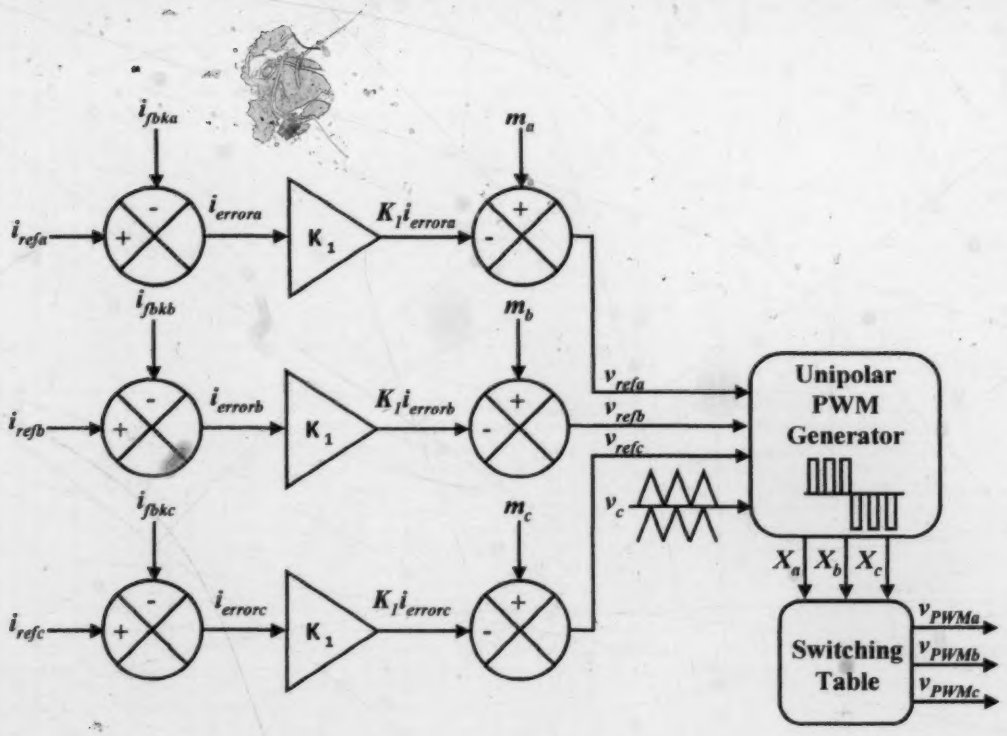


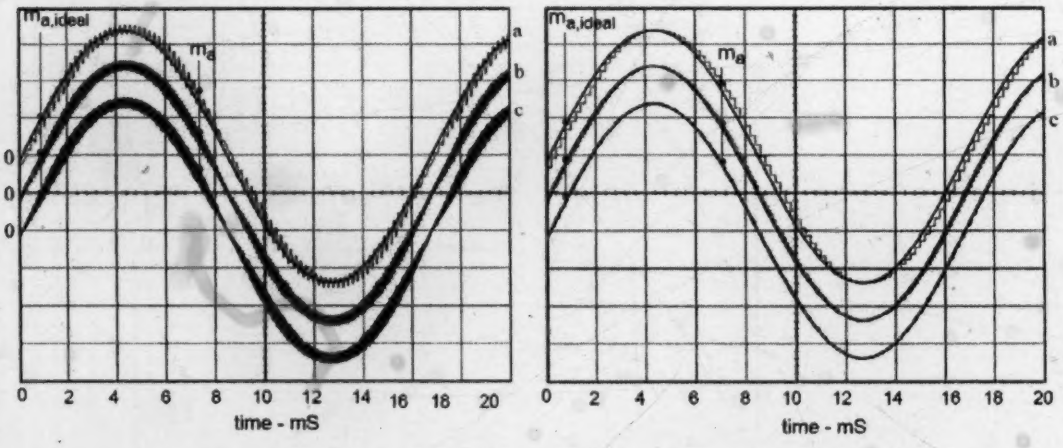
Figure 3.10: Proposed dual current control technique

3.6 Generating the m_a Signal for the Proposed Single Phase Current Controller

In figure 3.5, the modulation depth signal is produced by the feedback of the supply voltage. Due to the voltage drop across the supply inductance, the modulation depth signal is slightly phase lagged from the supply voltage; however, the ideal modulation depth signal is difficult to generate directly from the supply voltage feedback. Equation (3.5) states the average of the PWM signal is equivalent to the magnitude of the modulation depth signal for any arbitrary hysteresis band and integration constant. Subsection 3.2 concludes that the average of the PWM signal is approximately equal the magnitude of the modulation depth signal for a carrier-based closed-loop system since variations in the integration constant has minimal effect on PWM signal generation.

In general, the average of the PWM signal can be obtained in two ways: Sample and Hold circuits, which samples the average of the PWM signal at twice the carrier frequency, or a second order low pass Butterworth filter designed for -20dB attenuation frequency relative to the carrier frequency. The purpose of sample and hold circuitry is to take a snapshot of the signal at a specific time frame and hold that value. Sample and

hold approach is the fastest technique for acquiring the average of the PWM signal yet it is complex in nature and requires extensive design for proper operation. In contrast, 2nd order low pass Butterworth filter provides simple and easy means of obtaining the modulation depth signal. Figure 3.11 compares the quality of the two techniques for generating the modulation depth signal.



a)m_a: 2nd order LP Butterworth filter with $f_{20dB} = f_c$ b) m_a: SH filter averaging at $f_{SH} = f_c$

Key: a- f_c = 2.5kHz, b- f_c = 5kHz, c- f_c = 10kHz (at Ls = 5mH, Vs = 120V, V_{DC} = 200V)

Figure 3.11: Comparison of SH and 2nd order LP Butterworth filter for generating m_a

From figure 3.11, it is apparent that a 2nd order low pass Butterworth filter provides a suitable means of generating a modulation depth signal from a unipolar PWM signal with performance similar to the one provided by sample and hold technique. The phase shift of the modulation depth signal depends on the value of the supply inductance; however, the phase of modulation depth signal approaches $m_{a,ideal}$ as the carrier frequency is increased.

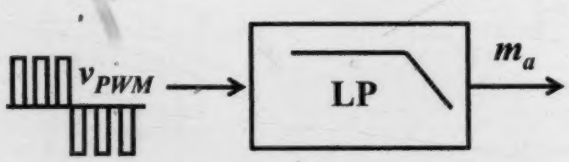


Figure 3.12: Single phase m_a generation

Note that it is not necessary to use a Butterworth low pass filter for obtaining the average of the PWM signal. Various filter classes, such as Chebyshev and Bessel filters, exist and can be utilized instead of Butterworth filters. However, Butterworth filters provide the flattest pass band and introduce small phase shifts for the pass-band compared with other conventional filters.

3.7 Generating Modulation Depth Signals for Proposed Three Phase Current Control and 2-Current Control Techniques

In the proposed single phase current controller, the feedback of the unipolar PWM signal through a 2nd order low pass Butterworth filter (designed for $f_{20dB} = f_c$) is sufficient for generating the modulation depth signal. In a three phase system, the phase voltages are not independent of each other due to mutual coupling between the three phases. Each phase voltage is composed of portions from the other phase voltages.

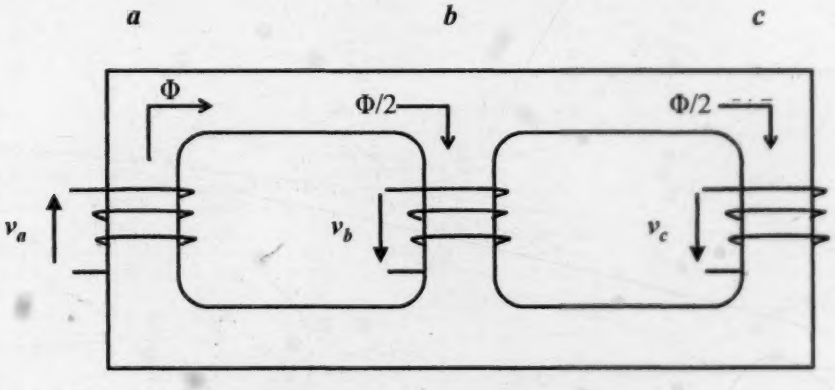


Figure 3.13: Wye connected three phase system

Imagine voltage v_a is applied to phase a in the system illustrated above. The applied voltage will result in the generation of flux which flows out of phase "a" and into phase "b" and phase "c". The flow of flux into phase "b" and phase "c" will induce voltages v_b and v_c in the respective phases. Thus, the voltage of phase "a" is composed of the applied voltage v_a as well as the sum of induced voltages v_b and v_c. Due to the interference between the three phases, a simple feedback of the unipolar PWM signals is not sufficient for obtaining the proper sinusoidal modulation depth signals. These phase

interactions can be minimized by compensating for the addition of the other two phases in the PWM signals. Consider only phase "a" in figure 3.13, with v_b and v_c are projected along phase "a".

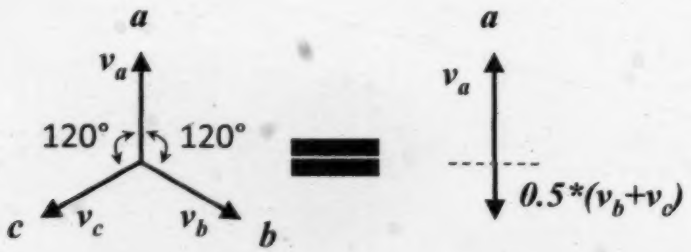


Figure 3.14: Three phase voltage vectors

The resulting voltage signal projected along phase "a" is given by:

$$v_{pha} = v_a - \frac{1}{2}(v_b + v_c) \tag{3.11}$$

In a balanced three phase system, the sum of all three phase voltages is equal to zero.

$$v_a + v_b + v_c = 0 \Rightarrow v_a = -(v_b + v_c) \tag{3.12}$$

Substituting equation (3.12) into equation (3.11) yields:

$$v_{pha} = v_a + \frac{1}{2}v_a = \frac{3}{2}v_a \tag{3.13}$$

$$v_{pha} = K \times v_a \Rightarrow v_a = \frac{v_{pha}}{K}; \qquad K = \frac{3}{2} \tag{3.14}$$

Substituting equation (3.14) into (3.11), voltage v_a can be represented by the following equation:

$$v_a = \frac{2}{3}v_a - \frac{1}{3}v_b - \frac{1}{3}v_c \tag{3.15}$$

Results for the other two phases can be obtained using a similar procedure. Applying this method to unipolar PWM signals, the modified PWM feedback signals are given by the following expressions:

$$v_{PWM\,A} = \frac{2}{3}v_{PWM\,a} - \frac{1}{3}v_{PWM\,b} - \frac{1}{3}v_{PWM\,c} \tag{3.16}$$

$$v_{PWM\,B} = \frac{2}{3}v_{PWM\,b} - \frac{1}{3}v_{PWM\,a} - \frac{1}{3}v_{PWM\,c} \tag{3.17}$$

$$v_{PWM\,C} = \frac{2}{3} v_{PWM\,c} - \frac{1}{3} v_{PWM\,a} - \frac{1}{3} v_{PWM\,b} \quad (3.18)$$

The modulation depth signals (m_a, m_b, and m_c) are obtained by feeding back the modified unipolar PWM signals ($v_{PWM\,A}$, $v_{PWM\,B}$, $v_{PWM\,C}$) through their respective 2nd order low pass Butterworth filters. The compensation for phase interactions allows the low pass filters to be designed for f_{20dB} equal to twice the carrier frequency; this has the benefit of reducing the phase shift between the modulation depth signals and their respective phase voltages thus resulting in lower distortions in the line currents.

Conversely, the 2-current control scheme does not rely upon the use of modified unipolar PWM signals for obtaining modulation depth signals. The general sub-topology illustrated in figure 3.8 is directly linked to the actual rectifier topology. When the sub-topology is operated as a stacked dual boost rectifier, the proposed dual current controller automatically compensates for phase interactions due to the nature of its design. As such, a simple feedback of the unipolar PWM signals (v_{PWMa}, v_{PWMb}, v_{PWMc}) through 2nd order low pass filters is sufficient for obtaining the modulation depth signals m_a, m_b, and m_c.

3.8 Determining K_1 for the Proposed Single Phase Current Controller

The high frequency ripple of the voltage reference signal (v_{ref}) can be directly related to the ripple in the current error signal. This relationship is expressed in the following equation:

$$v_{ref} = m_a - K_1 \times i_{error} \quad (3.19)$$

From equation (3.14) it is observed that the modulation depth signal provides the fundamental component of the voltage reference signal while the peak-to-peak ripple is proportional to the peak-to-peak ripple of the current error signal multiplied by proportional gain constant K_1. If either the current error ripple or K_1 is too large, v_{ref} can ramp faster than the carrier signal leading to loss of control and general instability of the controller. Conversely, if the peak-to-peak current error ripple is too small (or alternatively, K_1 is too small), accurate control of the line current is lost leading to a large fundamental component in the current error signal. Successful implementation of the proposed single phase current control technique depends on the appropriate choice of the proportional gain constant K_1. This section provides the design guidelines necessary for

selecting the proper proportional gain constant for the proposed single phase current control scheme. The analysis assumes dimensionless signal magnitudes and a carrier signal, with frequency f_c, ramping between ±1.

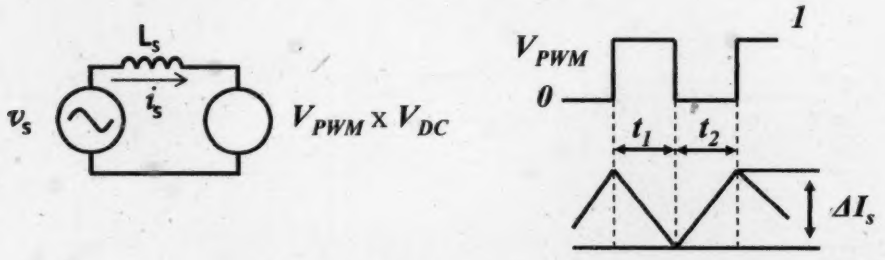


Figure 3.15: The AC input side of PWM rectifier

When the supply current is in the positive half cycle, V_{PWM} operates with positive unipolar PWM going from 0 to V_{DC} at twice the carrier frequency. Neglecting changes in the demand current and the supply voltage, the voltage drop across the inductor can be defined as:

$$v_s - v_{PWM} \times V_{DC} = L_s \frac{di_s}{dt} = v_L \tag{3.20}$$

$$\text{At } t = t_1\text{: } V_{PWM} = 1 \Rightarrow V_s - V_{DC} = -L_s \frac{\Delta I_s}{t_1} \tag{3.21}$$

$$\text{At } t = t_2\text{: } V_{PWM} = 0 \Rightarrow V_s = L_s \frac{\Delta I_s}{t_2} \tag{3.22}$$

Equating (3.21) and (3.22) with respect to V_s yields:

$$L_s * \Delta I_s \left(\frac{1}{t_1} + \frac{1}{t_2} \right) = V_{DC} \tag{3.23}$$

For unipolar PWM, it is known that $t_1 = \frac{\delta}{2f_c}$ and $t_2 = (1-\delta)\frac{1}{2f_c}$, where δ is the ratio of the pulse on-time over its entire period (i.e. duty cycle). Equation (3.5) states that the duty cycle of a PWM signal is equivalent to the modulation depth signal. Using this relationship, equation (3.23) can be expressed as:

$$\Delta I_s = \frac{V_{DC}}{2f_c L_s} * m_a (1 - m_a) \tag{3.24}$$

Since $\Delta v_{ref} = \Delta(K_1 \times i_{error}) = K_1 \times \Delta i_{error} = K_1 \times \Delta I_s$, equating equations (3.8) and (3.24):

$$\frac{R}{2f_c} * m_a(1-m_a) = K_1 * \frac{V_{DC}}{2f_c L_s} * m_a(1-m_a) \tag{3.25}$$

$$R = K_1 \frac{V_{DC}}{L_s} \tag{3.26}$$

For a given base ramping rate (R) for v_{ref}, Δv_{ref} is maximized when $m_a = 0.5$:

$$\Delta v_{ref,\ max} = \frac{R}{8f_c} \tag{3.27}$$

$$\Delta I_{s,\ max} = \frac{\Delta v_{ref\ max}}{K_1} = \frac{V_{DC}}{8f_c L_s} \tag{3.28}$$

From figure 3.4 (a), the maximum value for R should be $|4 \times f_c|$ to ensure the maximum ramping rate of v_{ref} does not exceed the carrier slope. Thus, R = $4f_c$ allows for wide operation range while R > $4f_c$ typically results in a loss of control and general instability. Therefore, for R = $4f_c$:

$$\Delta I_{s,\ max} = \frac{4f_c}{8K_1 f_c} = \frac{1}{2 \times K_1} \Rightarrow K_1 = \frac{4f_c L_s}{V_{DC}} \tag{3.29}$$

3.9 Determining K_1 for the Proposed Three Phase Current Control Techniques

In the proposed three phase current control technique and the subsequent 2-current control technique, proportional gain factor K_1 for each of the three phases is same. Thus, the analysis of determining a suitable K_1 value is simplified when only considering one phase. This section provides the design guidelines necessary for selecting the proper proportional gain constant for the proposed three phase current control schemes. For a balanced three phase supply:

$$V_a + V_b + V_c = 0 \tag{3.30}$$

$$I_a + I_b +_c = 0 \tag{3.31}$$

Assuming no change in the three phase supply voltages and the demand currents, the magnitude of the supply voltages and the line currents are given by:

$$|V_a| = |V_b| = |V_c| = V_s \tag{3.32}$$

$$|I_a| = |I_b| = |I_c| = I_s \tag{3.33}$$

During the positive half cycle of the line currents, the rectifier input voltage forms a three level unipolar PWM waveform switching at the carrier frequency. Assuming $L_a = L_b = L_c = L_s$, the voltage drop across the line inductors is given by:

$$v_s - v_{PWM} \times V_{DC} = L_s \frac{di_s}{dt} = v_L \tag{3.34}$$

At $t = t_1$: $V_{PWM} = 1 \Rightarrow V_s - \frac{1}{3} V_{DC} = -L_s \frac{\Delta I_s}{t_1}$ (3.35)

At $t = t_2$: $V_{PWM} = -1 \Rightarrow V_s + \frac{1}{3} V_{DC} = L_s \frac{\Delta I_s}{t_2}$ (3.36)

Equating (3.21) and (3.22) with respect to V_s yields:

$$L_s * \Delta I_s \left(\frac{1}{t_1} + \frac{1}{t_2} \right) = \frac{2}{3} V_{DC} \tag{3.37}$$

Where $t_1 = \delta T_{rect}$, $t_2 = (1 - \delta) T_{rect}$ and δ is the ratio of the pulse on-time over its entire period (i.e. duty cycle). Equation (3.5) states that the duty cycle of a PWM signal is equivalent to the modulation depth signal. Using this relationship, equation (3.37) can be expressed as:

$$\Delta I_s = \frac{2}{3} \frac{V_{DC}}{f_c L_s} * m_a (1 - m_a) \tag{3.38}$$

Since $\Delta v_{ref} = \Delta (K_1 \times i_{error}) = K_1 \times \Delta i_{error} = K_1 \times \Delta I_s$, equating equations (3.8) and (3.38):

$$\frac{R}{2 f_c} * m_a (1 - m_a) = K_1 * \frac{2}{3} \frac{V_{DC}}{f_c L_s} * m_a (1 - m_a) \tag{3.39}$$

$$R = K_1 \frac{4}{3} \frac{V_{DC}}{L_s} \tag{3.40}$$

Δv_{ref} is maximized when $m_a = 0.5$:

$$\Delta v_{ref,\,max} = \frac{R}{8 f_c} \tag{3.41}$$

$$\Delta I_{s,\,max} = \frac{\Delta v_{ref\ max}}{K_1} = \frac{V_{DC}}{6 f_c L_s} \tag{3.42}$$

Similar to the proposed single phase controller analyzed in section 3.8, the maximum value for R should be $|4 \times f_c|$ to ensure the maximum ramping rate of v_{ref} does not exceed the carrier slope. Therefore, for R = $4f_c$:

$$\Delta I_{s,\max} = \frac{4f_c}{8K_1 f_c} = \frac{1}{2 \times K_1} \Rightarrow K_1 = \frac{3f_c L_s}{V_{DC}} \tag{3.43}$$

3.10 Naturally Sampled Phase Disposition (PD) PWM Modulation

In the proposed single phase control scheme, a basic unipolar sinusoidal modulation strategy described in Chapter 1 is sufficient for obtaining good quality current control with low harmonic content. Using a similar modulation technique in the proposed three phase current control scheme yields poor control with large harmonic distortions. Thus, the proposed three phase schemes use a modulation technique known as naturally sampled phase disposition (PD) PWM [21-25]. This is a popular technique in multiphase applications due to its simplicity and a guarantee of good results in all operating conditions, including over-modulation [22].

For a three level rectifier, the available voltage levels are $+V_{DC}$, 0, and $-V_{DC}$. The boundaries between the different voltage levels are determined by the different modulation rules. From [22], it is known that for a three level system (N=3), N-1 = 2 carriers are needed. Thus for a naturally sampled PD PWM technique with N=3, the two carriers are arranged such that the phase difference between them is zero (Figure 3.16). For the three level system, the rectifier is switched to $+V_{DC}$ when the modulation signal is greater than both carriers. The rectifier switches to zero whenever the modulation signal is greater than the lower carrier but less than the upper carrier. Finally, the rectifier is switched to $-V_{DC}$ voltage level when the modulation signal is less than both carriers. This PWM scheme has an inherent advantage over traditional sinusoidal PWM modulation in such that no carrier harmonics are present [21, 22]. This consequently yields a lower THD in the supply current.

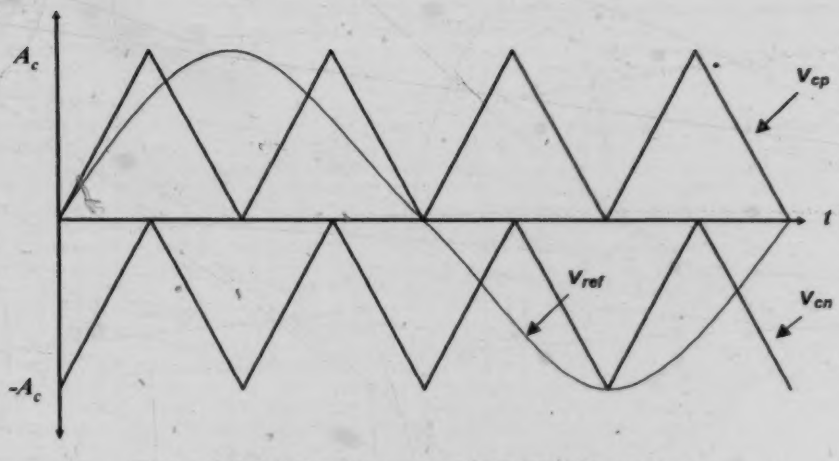


Figure 3.16: Naturally sampled PD PWM modulation

3.11 Summary

Basic ideas of combining the functionality of the hysteresis and carrier based current control are investigated through theoretical analysis of single and three phase PWM current control techniques. Two key factors for successful implementation of the propose current control schemes are the appropriate choice of K_1, which limits the peak-to-peak amplitude of the high frequency ripple in the current error signal, and the ability to generate an m_a signal which closely resembles the required ideal modulation depth signal. Generation of modulation depth signals for single and three phase proposed control schemes are discussed and theoretical analysis for determining the proportional gain factor for single and three phase cases is provided. This chapter sets the theoretical framework necessary for successful implementation of the proposed current control schemes.

Chapter 4 Single Phase Simulation Results for the Proposed Current Control Technique

Performance of the proposed single phase current controller is examined in steady-state and during transients using simulation results. Simulated results for single phase proportional-integral current controllers are also investigated for comparison purposes. Both control schemes are applied to PWM boost rectifiers and computer simulations are conducted to verify quality of the control; simulation models for the boost rectifiers are represented using discrete components instead of mathematical functions. Simulations are conducted assuming dimensionless signal magnitudes (i.e. per-unit system). The proposed current control scheme yields stable steady-state operation, quick transient responses with minimal overshoots, and an inherent tolerance to system disturbances such as DC offsets when compared to similarly tuned PI controllers.

4.1 Simulation Results for Single Phase PI Current Controller

Proportional-integral controllers are an industry standard for current control applications. While simple and inexpensive to implement, current control using PI compensators minimizes the error between the measured current and its respective reference value within a fixed frequency band. Transfer function for a PI compensator is given by:

$$T(s) = -\left(K_p + \frac{K_i}{s}\right) \tag{4.1}$$

The integral term (K_i) in the PI compensator generally improves the tracking by reducing the steady-state error while the proportion gain (K_p) affects the overall current error ripple. Basic block diagram of a PI current control scheme used for obtaining simulation results is illustrated in figure 4.1.

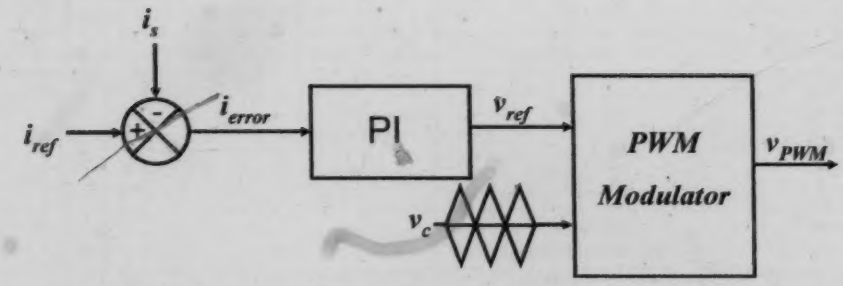


Figure 4.1: Single phase block diagram of PI current control scheme

From figure 4.1, the instantaneous current error (i_{error}) is fed to the PI compensator in order to produce the voltage reference signal (v_{ref}) for the PWM modulator. The voltage reference signal is compared with a triangle wave carrier ramping between ± 1, with a frequency f_c = 5 kHz, to generate the PWM switching signals. Successful implementation of this control scheme is highly dependant on the appropriate choices of K_p and K_i.

4.1.1 Steady State Operation of the Single Phase PI Current Controller

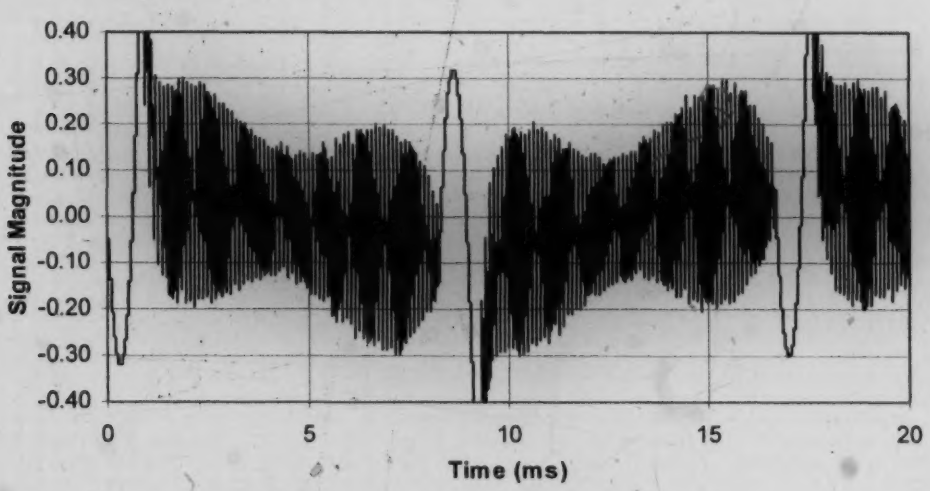
Analysis from Chapter 3 shows that best control for a carrier based current controller is achieved when the maximum peak-to-peak ripple of the scaled current error signal is 0.5. Linking the proportional gain of the PI compensator K_p to the gain factor K_1 from Chapter 3 ensures that the maximum peak-to-peak ripple for the scaled current error signal is equal to 0.5. Thus, for a single phase PWM boost rectifier with a supply voltage of 120 V, supply inductance at 5 mH, a peak current demand of 10 A, and a DC link voltage at 200 V, the peak-to-peak current ripple and the proportional gain are given by:

$$\Delta I_{s,\max} = \frac{V_{DC}}{8 f_c L_s} = \frac{200V}{8(5kHz)(5mH)} = 1A \tag{4.2}$$

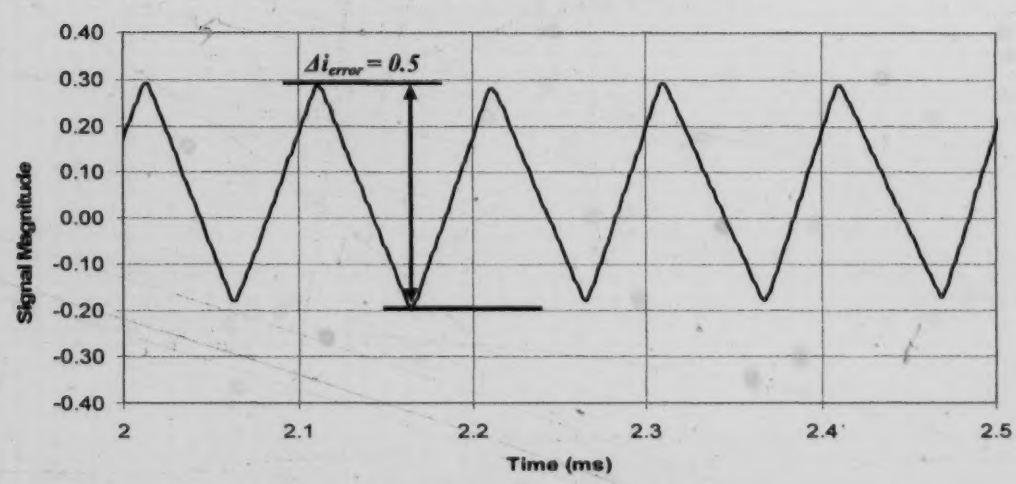
$$K_p = K_1 = \frac{4 f_c L_s}{V_{DC}} = \frac{4(5kHz)(5mH)}{200V} = 0.5A^{-1} \tag{4.3}$$

Figure 4.2 shows the maximum peak-to-peak ripple of the scaled current error for the single phase PI current control scheme; the integral gain K_i is arbitrarily selected to be equal to f_c to verify steady-state operation of the control. Figures 4.3 (a)-(b) illustrate the steady-state supply current waveform over one fundamental cycle and an expanded view

of the supply current showing the peak-to-peak current ripple. From figure 4.2 (b), it is apparent that when the proportional gain is equal to 0.5 A^{-1}, the maximum peak-to-peak ripple on $-K_i i_{error}$ is 0.5. For the given operating conditions (with $K_i = f_c$), figure 4.3 (b) shows that the peak-to-peak current ripple is approximately 1A which coincides with the theoretical value from equation (4.2).

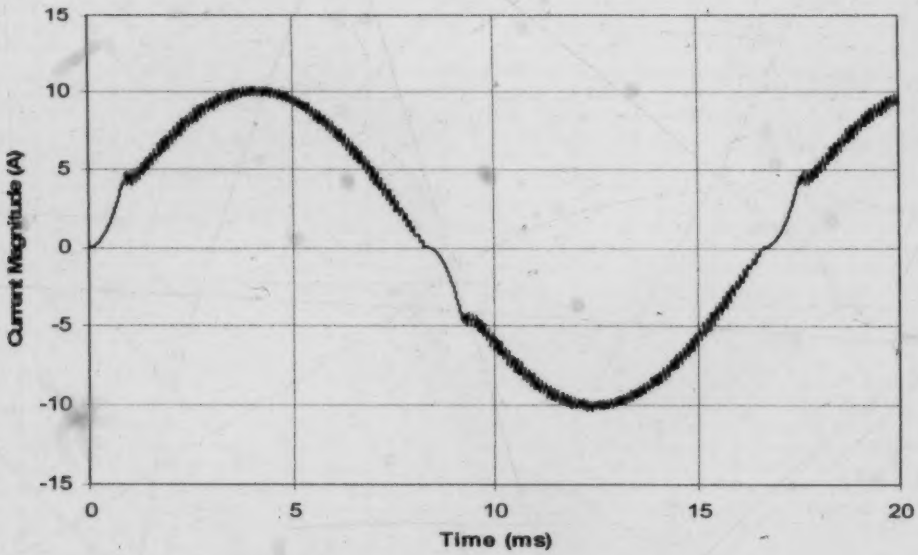


(a) $-K_i i_{error}$ signal in one fundamental period

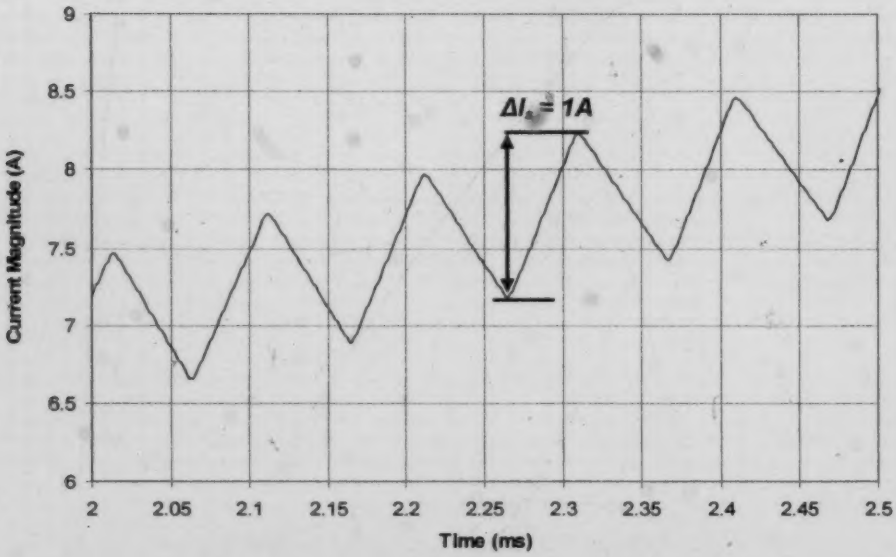


(b) Expanded view of $-K_i i_{error}$ signal

Figure 4.2: Peak-to-peak current error ripple for single phase PI current controller



(a) Supply current over one fundamental cycle



(b) Expanded view of the supply current waveform

Figure 4.3: Peak-to-peak current ripple for single phase PI current controller

4.1.2 Transient Analysis and Effects of K_i on the Steady-State Error

Transient analysis is vital for determining the stability of a controller. The ability to cope with sudden changes in demand current with a fast transient response and

minimal overshoots is a highly desirable feature in current control. A step change in the demand current is simulated to study the transient behaviour of the single phase PI current controller. The change of the demand current happens around the peak value of the supply current. The demand current is stepped down from 10A peak to 5A peak during the positive half cycle and the results are recorded for various K_i values. Simulation results of the transient response are illustrated in figure 4.4.

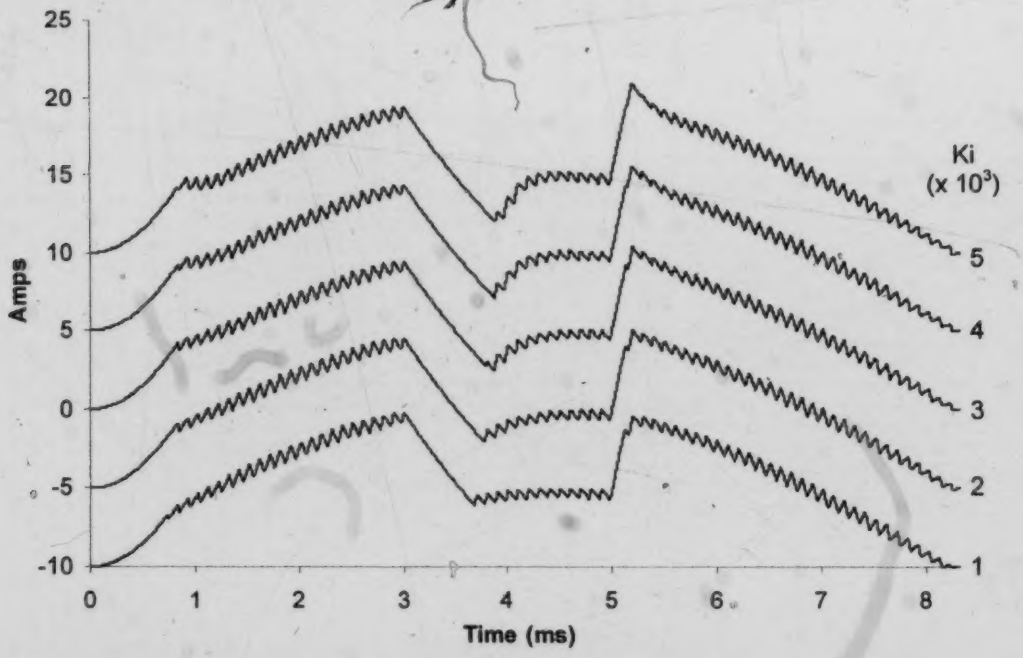


Figure 4.4: Offset waveforms: simulated transient response of single phase PI current controller

At higher integral gain values, a PI controller suffers from large overshoots during the transient. This is primarily due to the fact that the PI compensator integrates the large current error during the step change resulting in an under-damped response with large overshoots. The transient response can be significantly improved by lowering the integral gain but the steady-state current error gets worse (see figure 4.5).

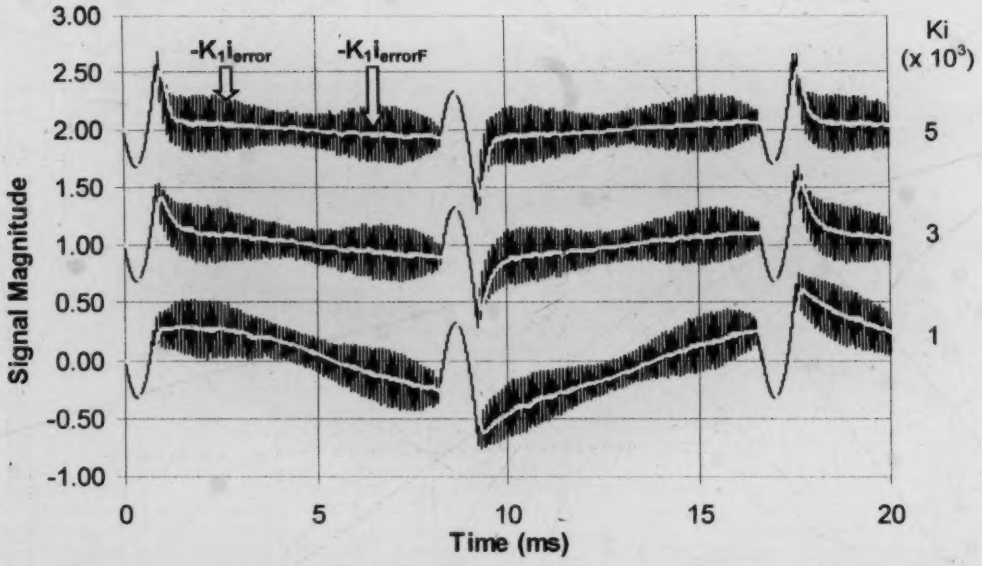


Figure 4.5: Offset waveforms: effect of K_i on single phase PI current controller steady-state current error

From figure 4.5, it is evident that a low integral gain yields a large steady-state current error; the quality of the current control suffers at small values of K_i. Consequently, when tuning a PI controller, one needs to ensure that a balance between large overshoots and small steady-state error is maintained.

4.2 Simulation Results for the Proposed Single Phase Current Control Scheme

Similar to a single phase current controller with PI compensators, the proposed single phase control scheme is simple and inexpensive to implement. This scheme utilizes the feedback of the unipolar PWM to force the average steady-state current error signal to zero (see Figure 3.5). The modulation signal (v_{ref}) for the PWM modulator is given by the following expression:

$$v_{ref} = m_a - K_1 \times i_{error} \tag{4.4}$$

From Chapter 3, the modulation depth signal m_a is generated by passing the unipolar PWM signal through a 2nd order low-pass Butterworth filter. The -20dB frequency (f_{20dB}) of the filter improves the current tracking by minimizing the steady-state

error while the proportional gain (K_1) affects the overall current ripple. The voltage reference signal is compared with a triangle wave carrier ramping between ± 1, with a frequency f_c = 5 kHz, to generate the PWM switching signals. Successful implementation of this control scheme is highly dependant on the appropriate choices of K_1 and f_{20dB}.

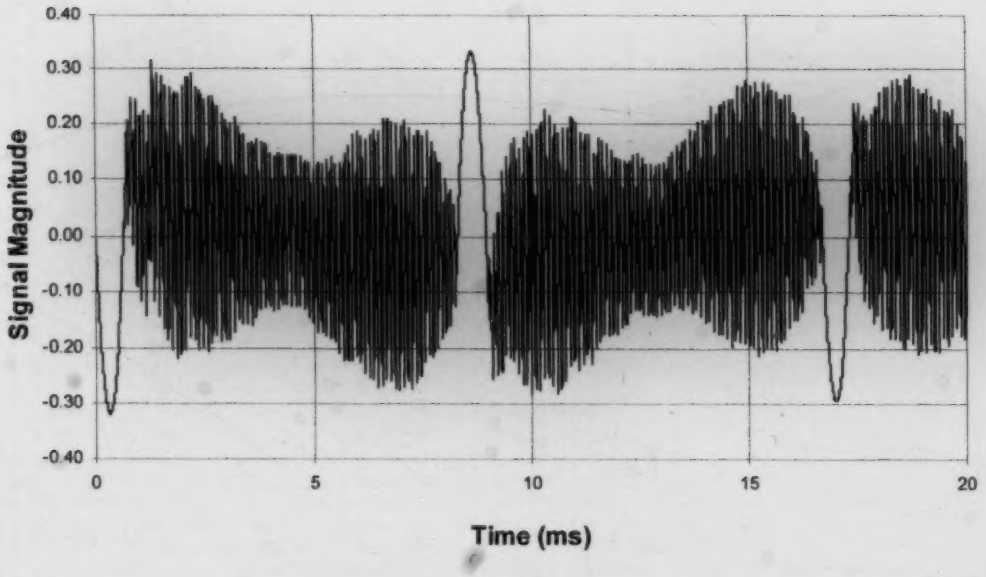
4.2.1 Steady State Operation of the Proposed Single Phase Current Control Scheme

Selecting an appropriate value for K_1 ensures best control performance by maintaining the maximum peak-to-peak ripple of the scaled current error signal at 0.5. Thus, for a single phase PWM boost rectifier operating with a supply voltage of 120 V, supply inductance of 5 mH, a peak current demand of 10 A, and a DC link voltage at 200 V, the peak-to-peak current ripple and the proportional gain in per-unit are given by:

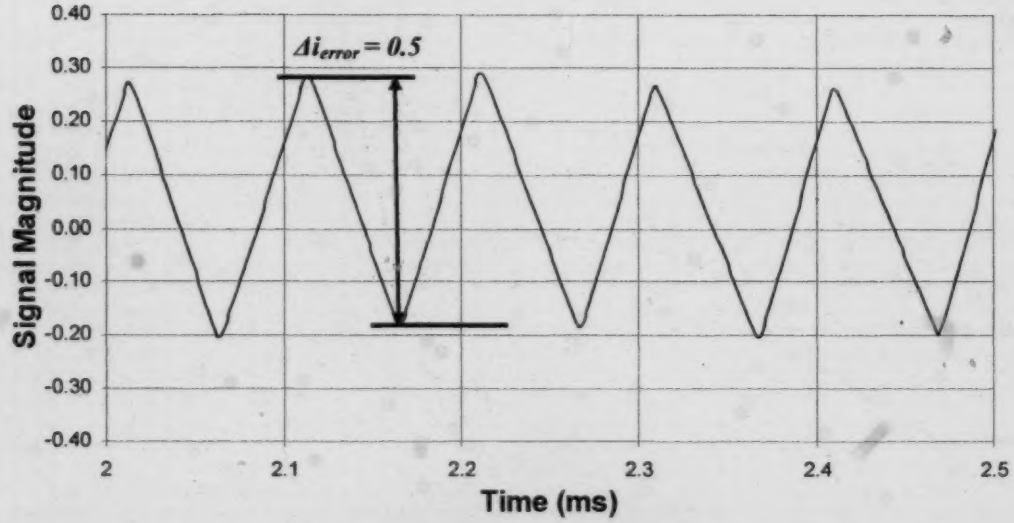
$$\Delta I_{s,\max} = \frac{V_{DC}}{8 f_c L_s} = \frac{200V}{8(5kHz)(5mH)} = 1A \tag{4.5}$$

$$K_p = K_1 = \frac{4 f_c L_s}{V_{DC}} = \frac{4(5kHz)(5mH)}{200V} = 0.5A^{-1} \tag{4.6}$$

Figure 4.6 illustrates the simulated maximum peak-to-peak current error ripple for the proposed single phase current control scheme; f_{20dB} is selected to be equal to f_c to verify steady-state operation of the control. Figures 4.7 (a)-(b) illustrate the steady-state supply current waveform over one fundamental cycle and an expanded view of the supply current showing the peak-to-peak current ripple. From figure 4.6 (b), it is apparent that for a proportional gain equal to $0.5A^{-1}$, the maximum peak-to-peak ripple on $-K_1 i_{error}$ is 0.5. For the given operating conditions (with $f_{20dB} = f_c$), figure 4.7 (b) indicates that the peak-to-peak current ripple is approximately 1A which coincides with the theoretical value from equation (4.5).

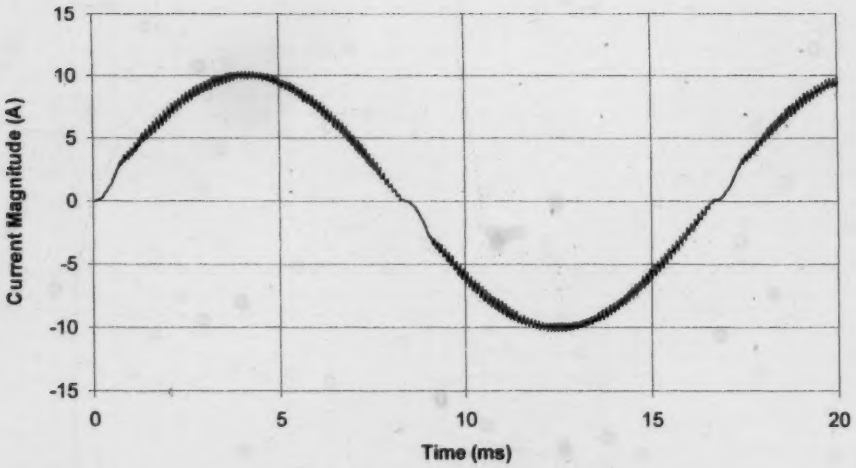


(a) $-K_I i_{error}$ signal in one fundamental period

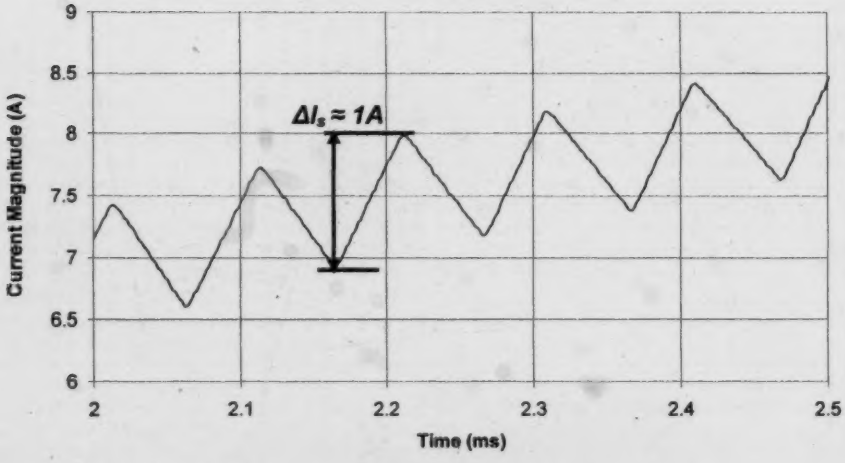


(b) Expanded view of $-K_I i_{error}$ signal

Figure 4.6: Peak-to-peak current error ripple for the proposed single phase current controller



(a) Supply current over one fundamental cycle



(b) Expanded view of the supply current waveform

Figure 4.7: Peak-to-peak current ripple for the proposed single phase current controller

4.2.2 Transient Analysis and Effects of f_{20dB} on the Steady-State Error

Transient analysis is conducted to analyze the stability of the proposed control scheme. A step change in the demand current is simulated to study the transient behaviour of the single phase PI current controller. The demand current changes at the peak value of the supply current. The demand current is stepped down from 10A peak to

5A peak during the positive half cycle and the results are recorded for various filter f_{20dB} values. Simulation results of the transient response are illustrated in figure 4.8.

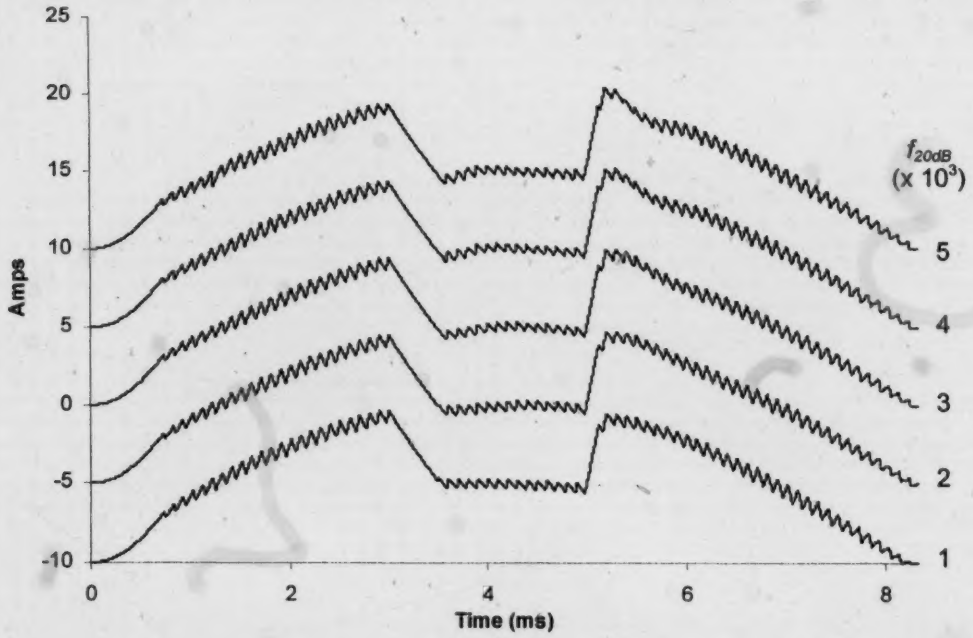


Figure 4.8: Offset waveforms: simulated transient response of the proposed single phase current controller

Figure 4.8 indicates a slight increase in current overshoots for higher values of f_{20dB}. However, the increase in the overshoots is not as drastic as those observed for increasing values of K_i in the PI current controller. The damped response of the proposed control scheme is advantageous in the sense that it allows for the use of higher values of f_{20dB} in order to minimize the steady-state current error. However, it should be noted that f_{20dB} values significantly greater than the carrier frequency lead to control instability. The transient response of the proposed single phase current control scheme can be improved by lowering the filter -20dB frequency at the cost of poor steady-state current error (see figure 4.9).

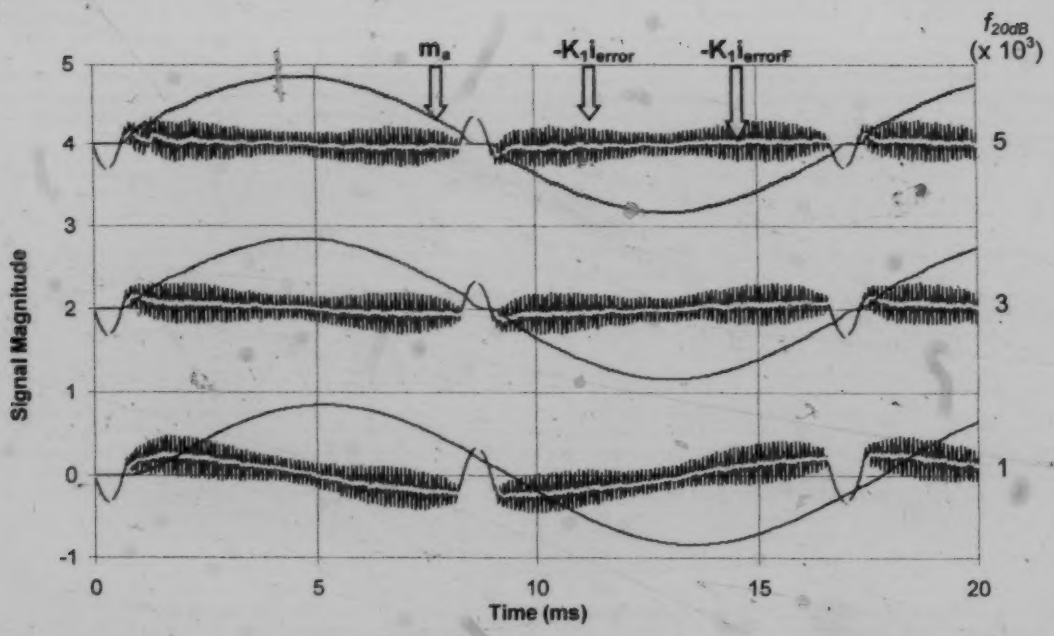


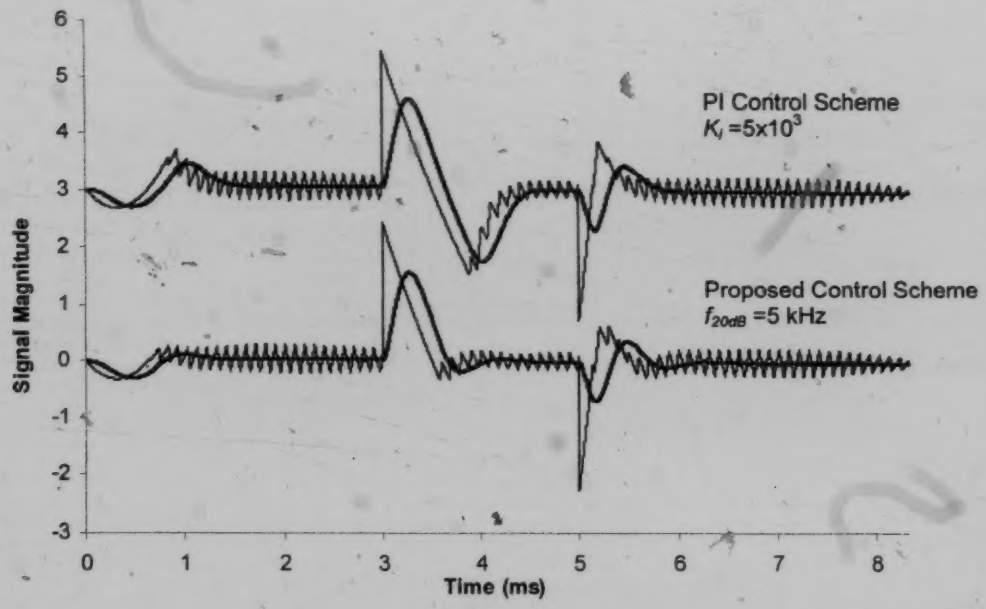
Figure 4.9: Offset waveforms: effect of f_{20dB} on the proposed single phase current controller steady-state current error

From figure 4.9, it is evident that a low -20dB frequency yields a larger steady-state current error; the quality of the current control suffers at small values of f_{20dB} due to a large fundamental frequency component in the current-error signal and a large phase shift in the modulation depth signal compared to $m_{a,\ ideal}$. The phase lag in the modulation depth signal decreases when f_{20dB} is increased, which helps in increasing the quality of the current control.

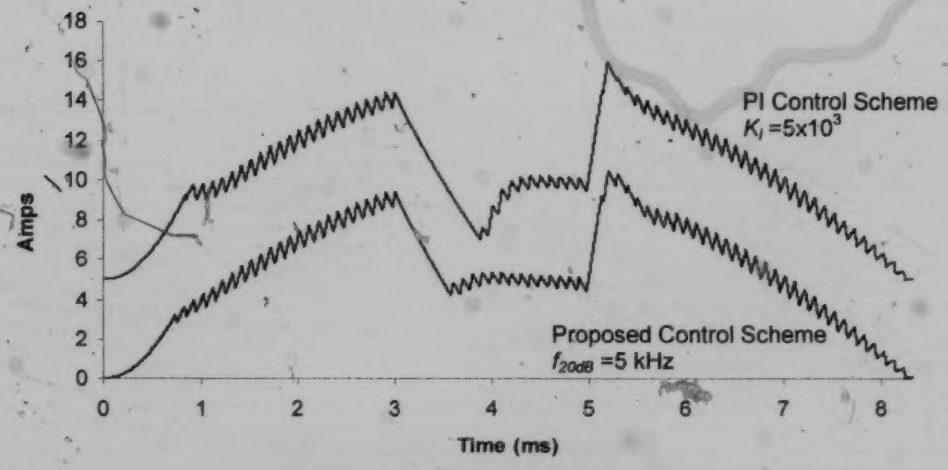
4.3 Comparison of Single Phase Current Control Schemes Using Simulation Results

From §4.1 and §4.2, it is observed that both the single phase PI current controller and the proposed single phase current control scheme can be tuned to give a wide range of control operation. Thus, for comparison purposes, both current control schemes need to be tuned to give similar performances. With an appropriate integral gain constant, the PI controller can achieve an average steady-state current-error similar to that for the proposed controller (compare figures 4.5 and 4.9). Simulation results comparing the transient response for the single phase PI current controller and the proposed single phase

current control scheme, when both schemes are tuned to obtain the same phase shift in the rectifier supply current and the same average steady-state current error, are shown in figure 4.10.



(a) $-K_I i_{error}$ and the average current error signal during a system transient



(b) Transient response of the supply current

Figure 4.10: Single phase offset waveforms comparing the controller response to a step change in the demand current

The simulation results in figure 4.10 show that the proposed single phase current controller has more stable transient response with smaller current overshoots. The damped transient response displayed by the proposed control scheme is very desirable in industrial processes which are highly sensitive to current overshoots.

Analog circuitry is prone to natural voltage offsets which can have adverse effects on a control scheme. Presence of offsets increases the complexity of the design since they need to be nullified or at the very least, compensated for. The ability of a current controller to tolerate such natural offsets in the system is a highly desirable feature. Consequently, DC offsets are introduced in the current reference signals of both control schemes in order to study their effect on the supply current. Simulation results in figure 4.11 illustrate the behaviour of the PI controller (when $K_i = 5x10^3$) under various offset conditions over a positive half cycle; figure 4.12 illustrates simulations results for the proposed single phase current control scheme (when f_{20dB} = 5 kHz) under similar offset conditions.

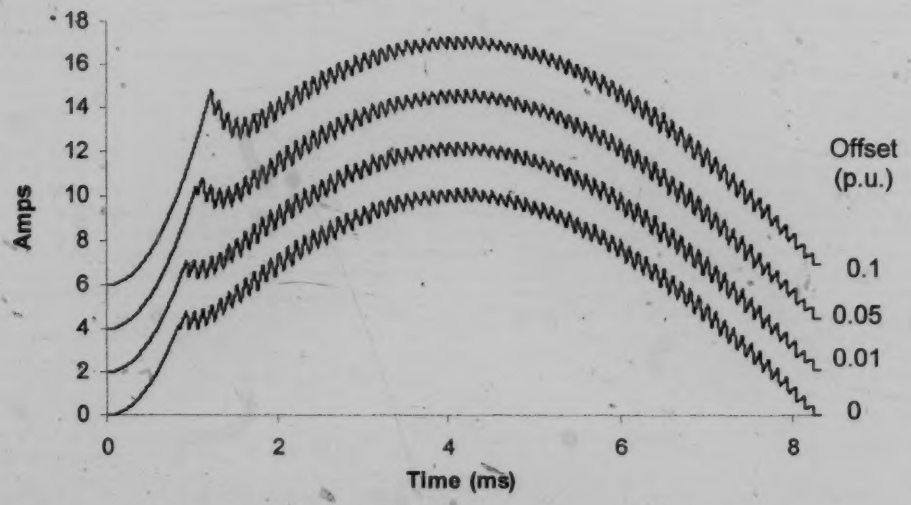


Figure 4.11: Offset waveforms: behaviour of single phase PI current control under DC offset conditions

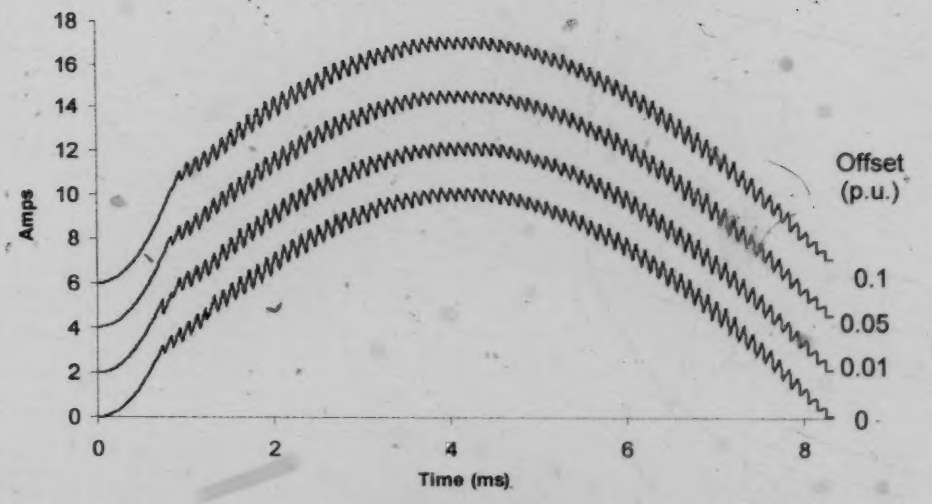


Figure 4.12: Offset waveforms: behaviour of the proposed single phase control scheme under DC offset conditions

DC offsets in the range of 100 mV and 500 mV are a common occurrence in analog control circuitry. From figure 4.11, it is clear that the presence of a DC offset in the current reference signal leads to a more oscillatory supply current due to the inability of the PI controller to cope minute system disturbances. This consequently limits the application of the single phase PI current control scheme as shown in figure 4.1. Compared to figure 4.11, simulation results in figure 4.12 display a more damped response to DC voltage offsets. This suggests that the proposed single phase current control scheme is better suited at coping with system disturbances like voltage offsets than then single phase scheme utilizing PI compensators. Taking into account the simulation results from this section and the previous sections, it can be safely concluded that the proposed current control scheme yields stable steady-state operation, quick transient responses with minimal overshoots, and an inherent tolerance to system disturbances such as DC offsets when compared to a similarly tuned PI controller.

4.4 Summary

Steady-state performance and the transient response of a single phase PI current controller and the proposed single phase current control scheme were tested using

computer simulations. Furthermore, the behaviour of both schemes was analyzed under system disturbance by introducing artificial DC voltage offsets in the current reference signals. The proposed current control scheme displayed superior performance compared to a PI control scheme in both the transient response and tolerance to system disturbances. The simulation results indicate that the proposed current control scheme yields stable steady-state operation, quick transient responses with minimal overshoots, and an inherent tolerance to system disturbances such as DC offsets when compared to a similarly tuned PI controller.

Chapter 5 Three Phase Simulation Results for the Proposed Current Control Techniques

Performance of the proposed three phase current controller technique and the 2-current control technique is examined under steady-state and during transients using computer simulations. Simulation results for a stationary frame PI current controller are also investigated for comparison purposes. All simulations are conducted on a three phase PWM boost rectifier assuming dimensionless signal magnitudes (i.e. per-unit). The proposed three phase current control technique and 2-current control technique yield stable steady-state operation, a quick transient response with minimal current overshoots, and an inherent tolerance to disturbances caused by phase interactions and DC offsets in the system when compared to a similarly tuned PI controller.

5.1 Simulation Results for a Stationary Frame PI Current Controller

Current controllers using PI compensators in the stationary reference frame are the most commonly employed current control schemes in three phase applications. Basic operation of this control scheme is described in §2.1.1 and a block diagram is presented in figure 2.1. This control scheme employs the use of three independent PI compensators to force the steady-state current error to zero. The behaviour of the PI compensators is the same regardless of whether it is applied in a single phase or three phase control scheme. The integral term is still responsible for minimizing the steady-state error while the proportional gain influences the overall current ripple. The modulation reference signals generated by the PI compensators are used to generate the PWM signals using the naturally sampled phase disposition PWM modulation scheme with a carrier frequency (f_c) equal to 10 kHz.

5.1.1 Steady-State Operation of the Stationary Frame PI Current Controller

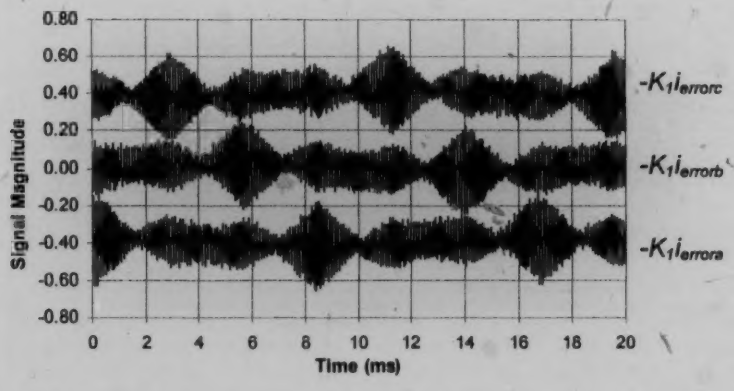
Similar to its single phase counterpart, the stationary frame PI current controller performs best when the maximum peak-to-peak ripple on the scaled current error signal is limited to 0.5. This is accomplished by choosing an appropriate value for the proportional gain. Linking the proportional gain of the PI compensators to the three

phase K_I factor from Chapter 3 ensures that the maximum peak-to-peak ripple in the scaled current error for all three phases is equal to 0.5. Thus, for a three phase PWM boost rectifier operating from star-connected three phase voltages with line inductances of 2.5 mH, peak current demand of 10 A, and a DC link voltage of 300 V, the peak-to-peak current ripple and the proportional gain in per-unit are given by:

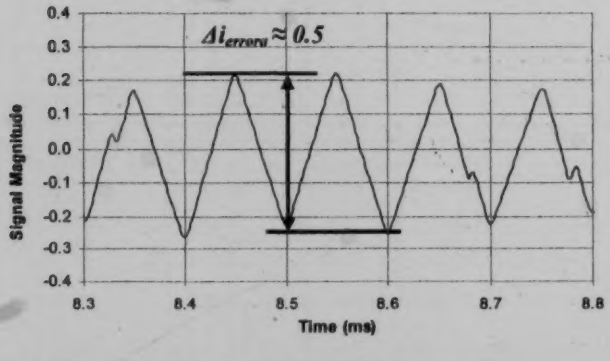
$$\Delta I_{s,\max} = \frac{V_{DC}}{6 f_c L_s} = \frac{300V}{6(10kHz)(2.5mH)} = 2A \tag{5.1}$$

$$K_p = K_1 = \frac{3 f_c L_s}{V_{DC}} = \frac{3(10kHz)(2.5mH)}{300V} = 0.25A^{-1} \tag{5.2}$$

Figure 5.1 (a) shows the steady-state current error for all three phases over an entire fundamental cycle for $K_i = 10\text{x}10^3$. An expanded view of $-K_1 i_{errora}$ is presented in Figure 5.1 (b).



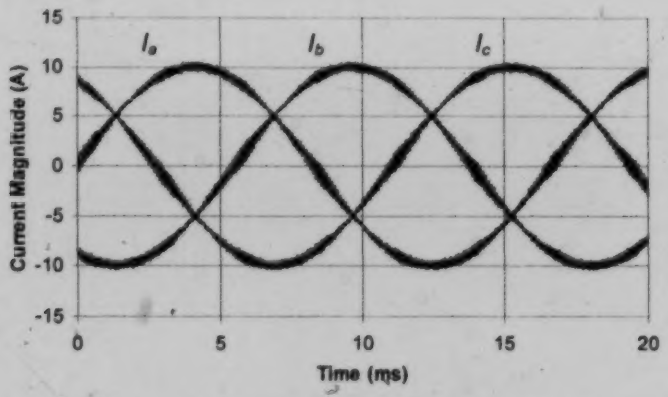
(a) Steady-state current error signals using $K_I = 0.25$ per-unit



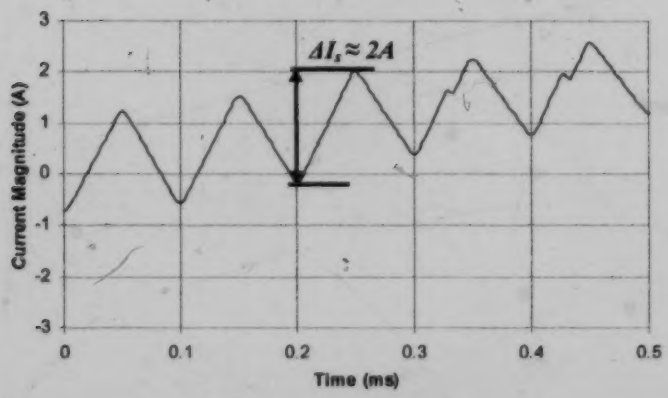
(b) Expanded view of $-K_1 i_{errora}$

Figure 5.1: Peak-to-peak current error ripple for the three phase PI current controller

Figure 5.1 (b) shows that for a proportional gain of 0.25, the maximum peak-to-peak ripple on the scaled current error is approximately 0.5. Figures 5.2 (a)-(b) illustrate the steady-state supply current waveform over one fundamental cycle and an expanded view of I_a showing the maximum peak-to-peak current ripple. For the given operating conditions (and $K_i = 10\text{x}10^3$), figure 5.2 (b) indicates that the maximum peak-to-peak current ripple on I_a is approximately 2A, which coincides with the theoretical value from equation (5.1). Note that the respective maximum peak-to-peak ripple on the current error signals and the supply currents are the same for all three phases; however, for the sake of simplicity, only expanded current error and supply current waveforms for phase "a" are provided.



(a) Three phase line currents over one fundamental cycle

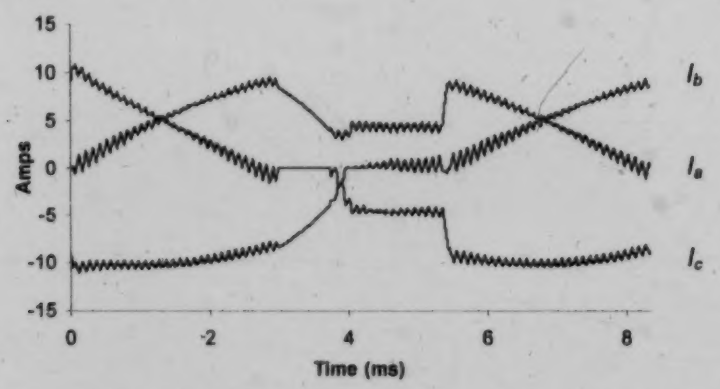


(b) Expanded view of I_a

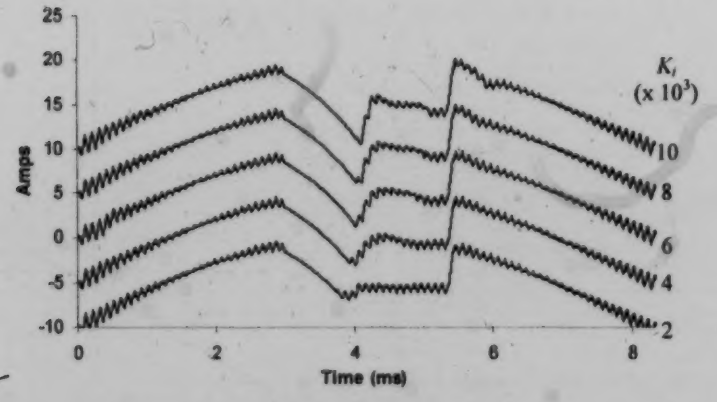
Figure 5.2: Peak-to-peak current ripple for the three phase PI current controller

5.1.2 Transient Analysis and Effects of K_i on the Steady-State Current Errors

A step change in the demand current for all three phases is simulated in order to study the transient behaviour of the stationary frame PI current controller. The step change occurs at the peak of the I_a and is also applied during the same time interval for I_b and I_c such that the transient occurs at the same time for all three phases. The demand current is stepped down by 50% (i.e. from 10A to 5A peak for I_a) and the results are recorded for various K_i values. Simulation results of the transient response are illustrated in figure 5.3. Figure 5.3 (a) shows the effect of the transient in all three phases. Figure 5.3 (b) shows the transient response of I_a for varying values of K_i.



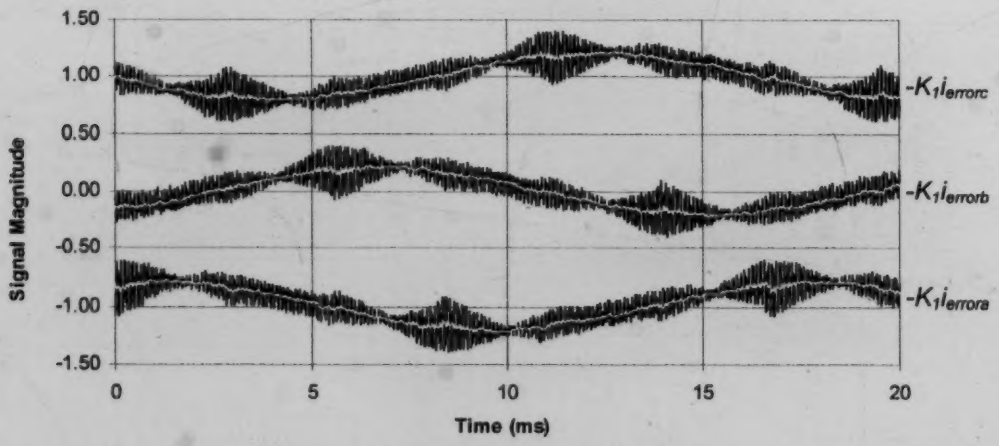
(a) Transient response showing all three phases ($K_i = 2x10^3$)



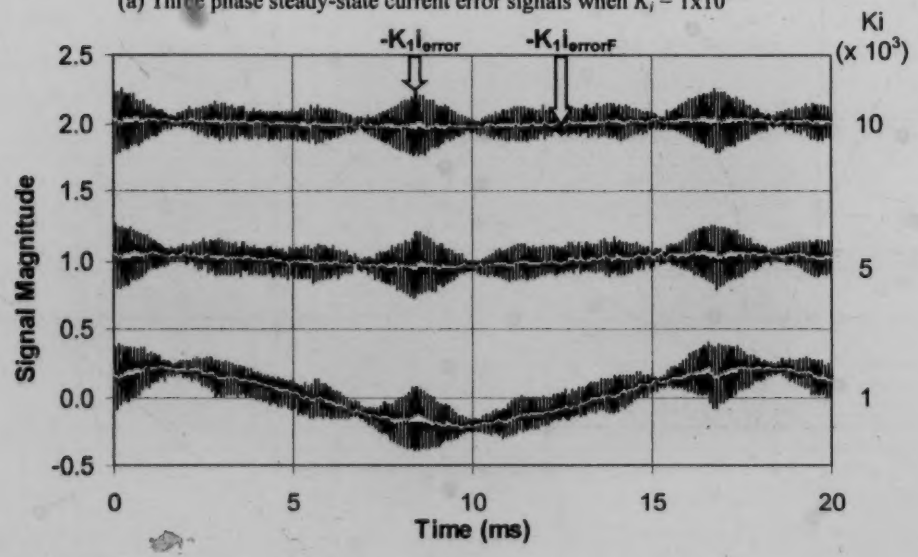
(b) Transient response of I_a for various K_i values

Figure 5.3: Offset waveforms: simulated transient response for the stationary frame PI current controller

Similar to its single phase counterpart, the stationary frame PI current controller suffers from large current overshoots for high values of K_i. The transient response can be significantly improved by lowering the integral gain, however, the fundamental component in the steady-state current error signals increases resulting in poor control quality. Figure 5.4 (a) shows the three phase current error signals for $K_i = 1x10^3$; figure 5.4 (b) illustrates the effect of the integral gain on the current error signals.



(a) Three phase steady-state current error signals when $K_i = 1x10^3$



(b) Effect of K_i on $-K_1 i_{errora}$

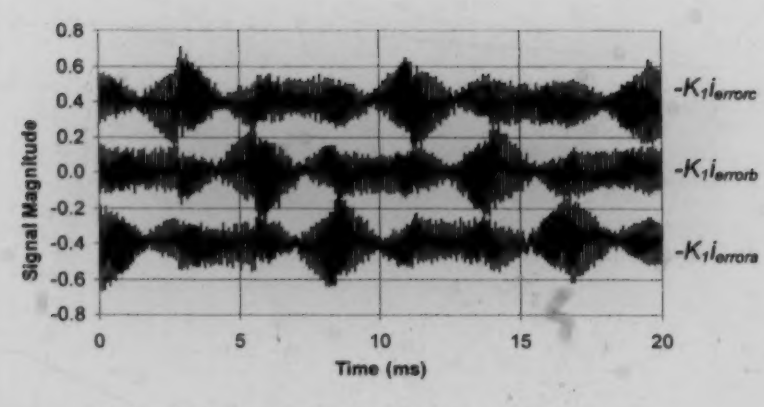
Figure 5.4: Offset waveforms: effect of Ki on the steady-state current error for the stationary frame PI current controller

5.2 Simulation Results for the Proposed Three Phase Current Control Technique

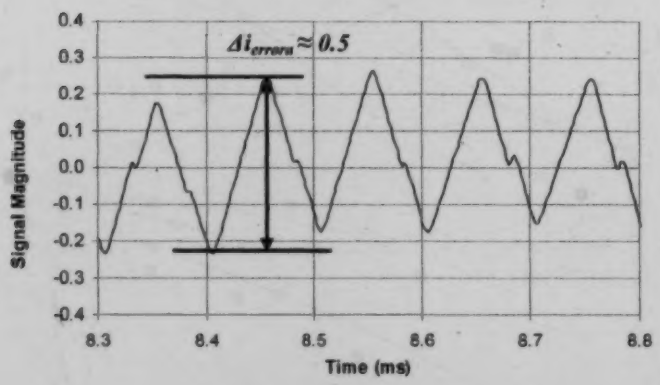
The basic operation of the proposed three phase current control scheme (3-current controller) is provided in §3.4 and the block diagram is presented in figure 3.6. This scheme relies on the feedback of modified unipolar PWM signals (v_{PWMA}, v_{PWMB}, v_{PWMC}) to minimize the steady-state current error signals. From Chapter 3, the modulation depth signals (m_a, m_b, m_c) are generated by passing the modified PWM signals through their respective 2nd order lowpass Butterworth filters. The f_{20dB} frequency of the filters improves current tracking by forcing the average current error signals to zero. This control scheme, like all other schemes presented in this chapter, utilizes the naturally sampled PD PWM modulation scheme with f_c = 10 kHz.

5.2.1 Steady-State Operation of the Propose Three Phase Current Controller

Limiting the maximum peak-to-peak current error ripple to 0.5 per-unit yields the best control performance. Given the same operating conditions as the three phase PWM boost rectifier in §5.1, the maximum peak-to-peak current ripple and the proportional gain value is given by equations (5.1) and (5.2). Figure 5.5 shows the steady-state current error for all three phases over an entire fundamental cycle for f_{20dB} = 20 kHz. Figure 5.5 (b) indicates that the maximum peak-to-peak ripple of the steady-state scaled current error signals is bounded between 0.5 when K_I = 0.25. Figure 5.6 illustrates the peak-to-peak current ripple of the three phase supply currents. Figure 5.6 (b) shows an expanded view of I_a indicating the $\Delta I_s \approx$ 2A.

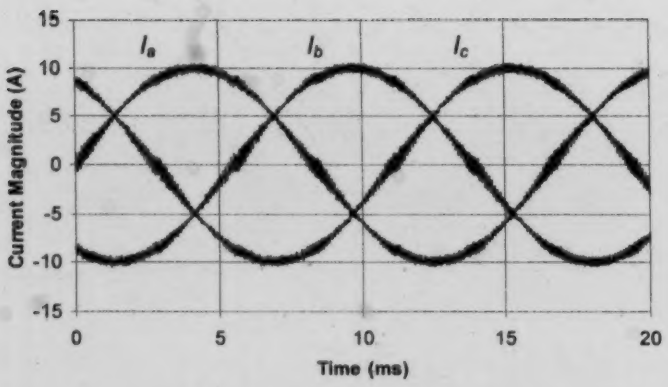


(a) Steady-state current errors using $K_1 = 0.25$ per-unit

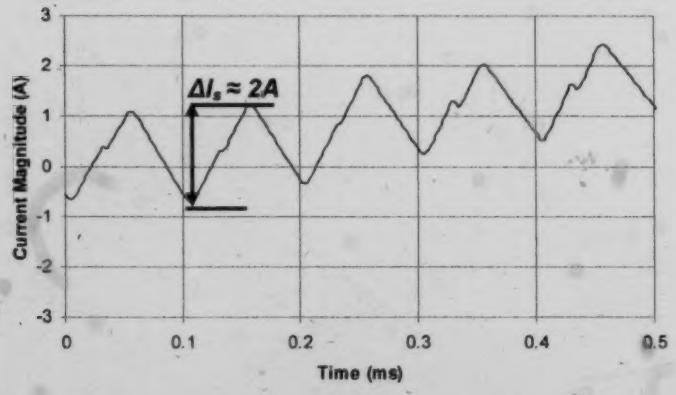


(b) Expanded view of $-K_1 i_{errora}$

Figure 5.5: Peak-to-peak current error ripple for the proposed three phase current controller



(a) Three phase line currents displayed over one fundamental cycle

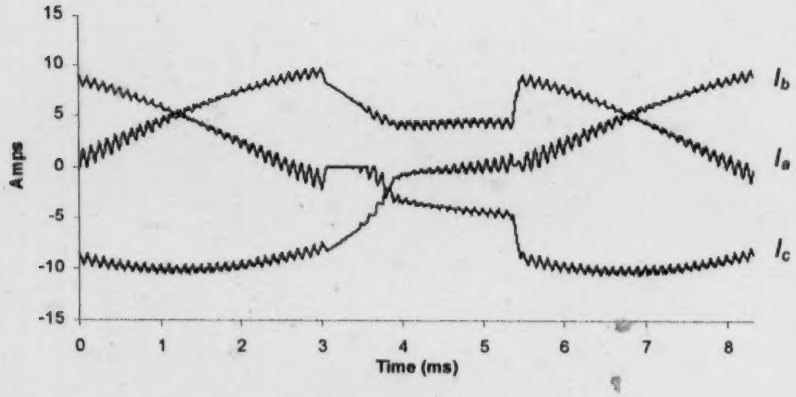


(b) Expanded view of I_a

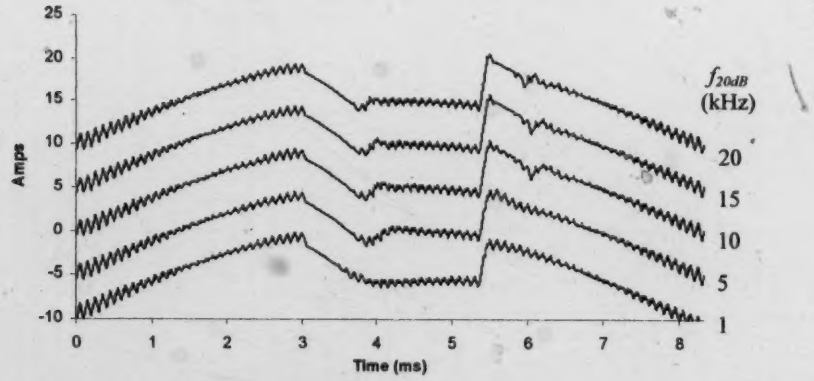
Figure 5.6: Peak-to-peak current ripple for the proposed three phase current controller

5.2.2 Transient Analysis and Effects of f_{20dB} on the Steady-State Current Errors

Transient response of the proposed three phase current control scheme is investigated using the procedure described in §5.1.2. Figure 5.7 (a) illustrates the effect of the transient in all three phase current waveforms. Figure 5.7 (b) shows the transient response of I_a for varying values of f_{20dB} frequency.



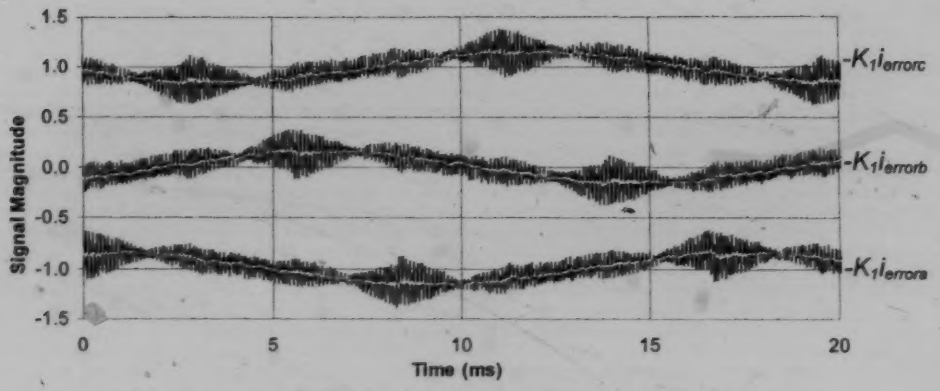
(a) Transient response showing all three phases (f_{20dB} = 1 kHz)



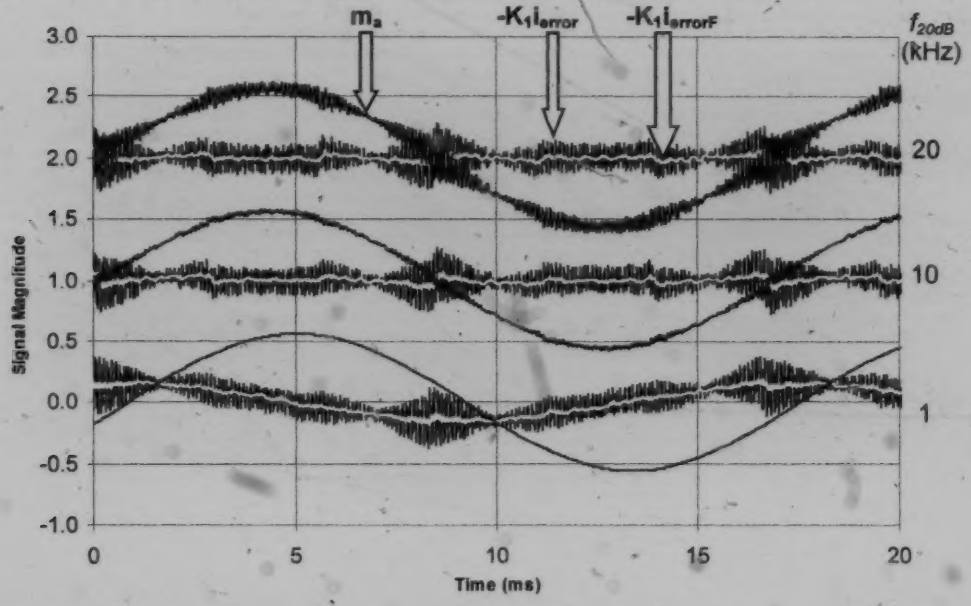
(b) Transient response of I_a for various f_{20dB} values

Figure 5.7: Offset waveforms: simulated transient response for the proposed three phase current controller

The proposed three phase current control scheme displays a more damped step response during the current transient as compared to the PI current control scheme. The relative current offshoot magnitudes remain constant for f_{20dB} values greater than 5 kHz; however, the low frequency distortion, which occurs at the 6 ms mark and only appears during a transient simulation, becomes more oscillatory for higher frequencies. This distortion is also present in the three phase PI controller for high values of K_i. Low frequency distortions in the current waveform can be eliminated by lowering the filter's f_{20dB}. Figure 5.8 shows the effect of lowering the -20dB frequency on the current error signals.



(a) Three phase steady-state current error signals when f_{20dB} = 1 kHz



(b) Effect of f_{20dB} on $-K_1 i_{errora}$

Figure 5.8: Offset waveforms: effect of f_{20dB} on the steady-state current error for the proposed 3-current controller

Although the current overshoots during the system transient can be minimized by the lowering the filter's -20dB frequency, the overall performance of the control suffers due to a large fundamental component in the current error signal (see figures 5.7 and 5.8 (a)). Furthermore, low values of f_{20dB} result in a larger phase shift in the modulation depth signals from their ideal cases (figure 5.8 (b)), which lead to poor control quality

and line currents that are not in phase with their supply voltages (i.e. non UFPF operation). However, when compared to a similarly tuned PI current controller, the proposed three phase current control scheme exhibits superior performance in terms of control stability and transient response.

5.3 Simulation Results for the Proposed 2-Current Controller

Section 3.5 describes the basic nature of this three phase current control scheme. During the dual current control mode, the PWM boost rectifier can be operated with star-connected bidirectional switches (see figure 3.7 (a)) or delta-connected bidirectional switches (see figure 3.7 (b)) depending on which configuration is required. The primary advantage of this control scheme is the reduced switching losses for the same average switching frequency when compared to the stationary frame PI current controller and the proposed three phase current control scheme. Utilizing a simple feedback of the unipolar PWM signals, this current control scheme is capable of providing a fast transient response and stable steady-state operation.

5.3.1 Steady-State Operation of the Proposed 2-Current Control Technique

Since the switching period of the semiconductor is only $2/3^{rd}$ of the overall switching period, the average switching frequency of the dual current controller is not equal to the average switching frequency of the proposed three phase current controller for the same carrier frequency. In order to obtain similar performance amongst the two schemes, the average switching frequencies need to be equal; hence a new carrier frequency for the 2-current control scheme needs to be obtained. For the 3-current control scheme, the average switching frequency is equal to the frequency of its carrier signal (f_c). For the 2-current control scheme however, the average switching frequency is given by the following expression:

$$f_{ave,\ dual} = \frac{2}{3} f_{c,\ dual} \tag{5.3}$$

Setting $f_{ave,\ dual}$ equal to the average switching frequency of the 3-current control scheme yields:

$$f_c = \frac{2}{3} f_{c,\ dual} \tag{5.4}$$

Thus, for f_c = 10 kHz, the frequency of the carrier signal used in the 2-current control scheme is given by:

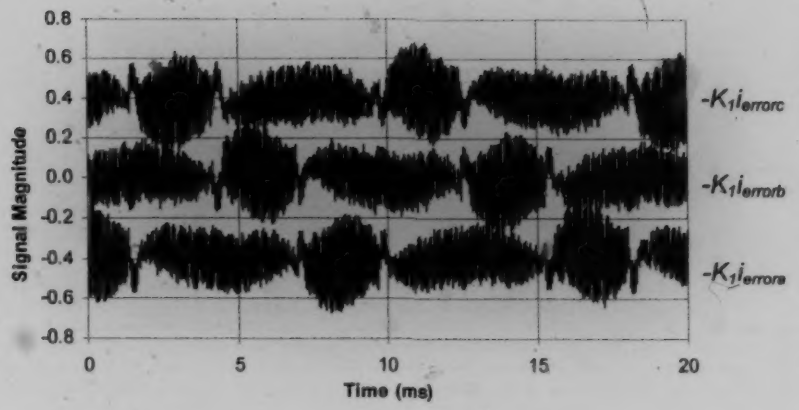
$$f_{c,\ dual} = \frac{3}{2} f_c = \frac{3}{2} \times 10kHz = 15kHz \tag{5.5}$$

Using the new carrier frequency for the 2-current controller and the operating conditions defined in §5.1, the maximum peak-to-peak current ripple and the proportional gain value is given by:

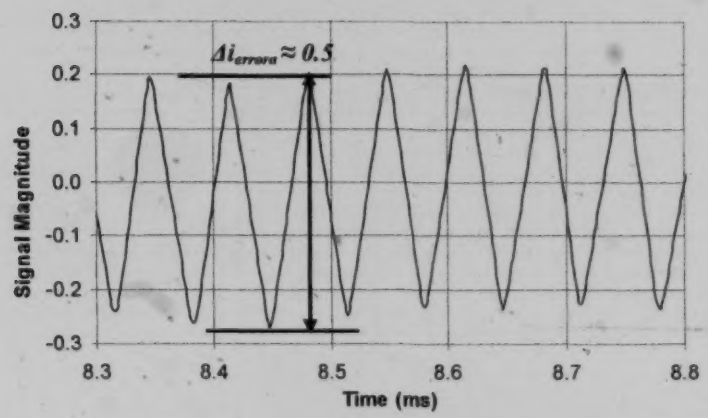
$$\Delta I_{s,\ \max} = \frac{V_{DC}}{6 f_c L_s} = \frac{300V}{6(15kHz)(2.5mH)} = 1.33A \tag{5.6}$$

$$K_p = K_1 = \frac{3 f_c L_s}{V_{DC}} = \frac{3(15kHz)(2.5mH)}{300V} = 0.375A^{-1} \tag{5.7}$$

Figure 5.9 (a) illustrates the steady-state current error signals for a star-connected bidirectional switch boost rectifier over an entire fundamental cycle. Figure 5.9 (b) shows the maximum peak-to-peak ripple on the scaled current error signal through an expanded view of $-K_1 i_{errora}$. Similarly, figure 5.10 (a) illustrates the steady-state current error signals for a delta-connected bidirectional switch boost rectifier with an expanded view of one of the waveforms presented in figure 5.10 (b).

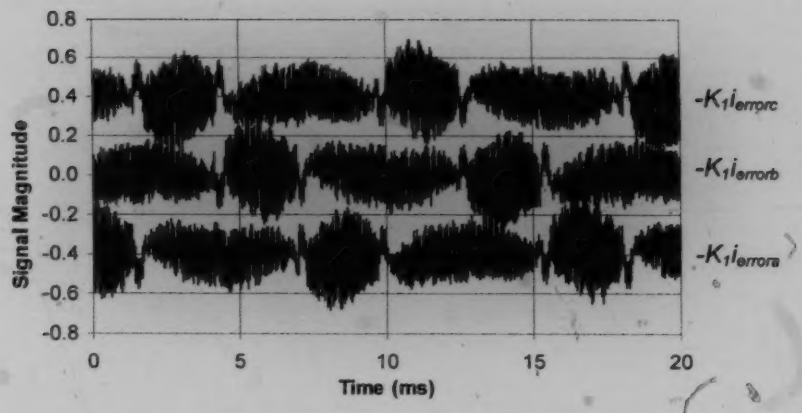


(a) Steady-state current errors using $K_1 = 0.375$ per-unit

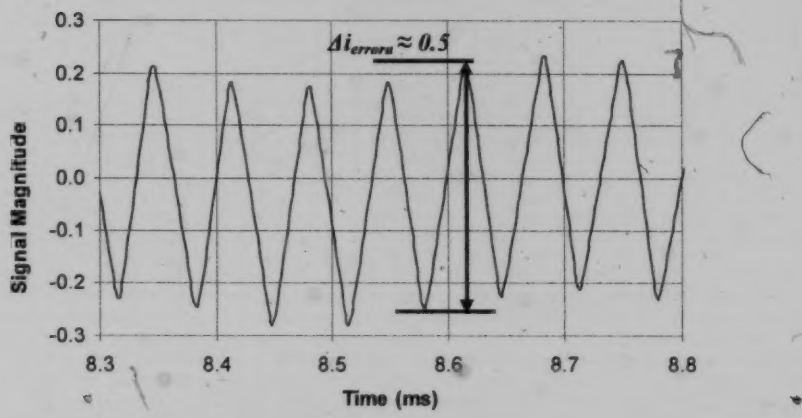


(b) Expanded view of $-K_1 i_{errora}$

Figure 5.9: Peak-to-peak current error ripple for the star-connected bidirectional switch rectifier operating under dual current control mode



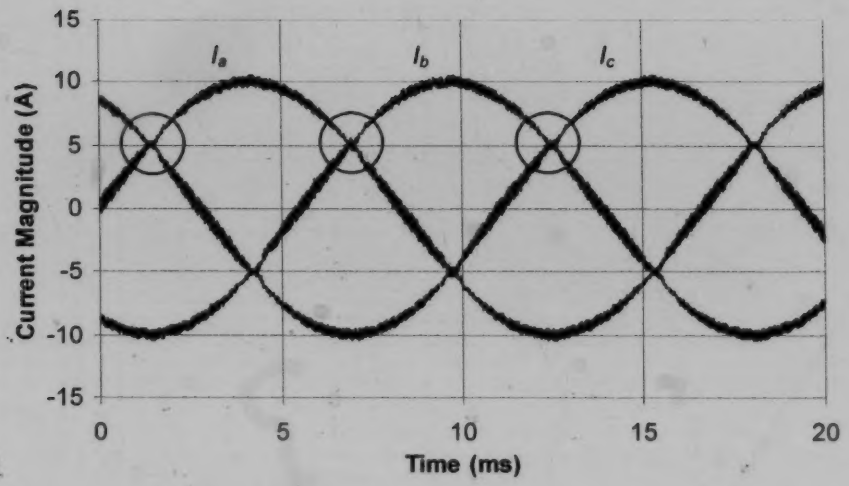
(a) Steady-state current errors using $K_1 = 0.375$ per-unit



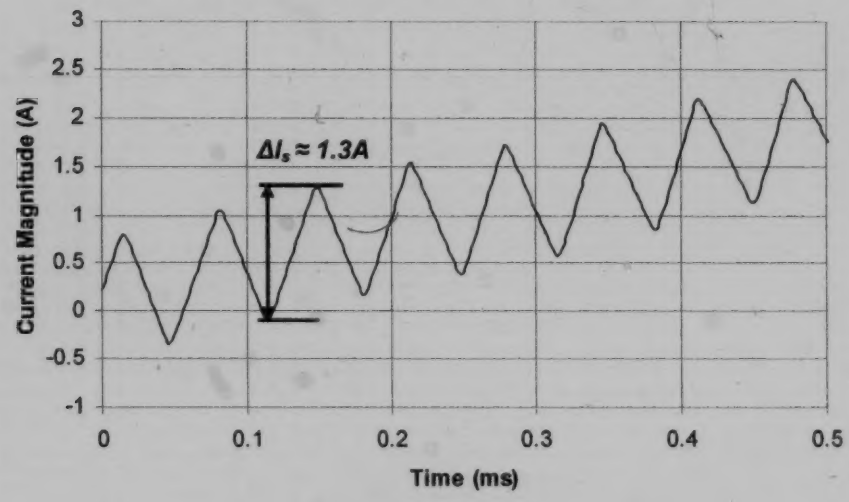
(b) Expanded view of $-K_1 i_{errora}$

Figure 5.10: Peak-to-peak current error ripple for the delta-connected bidirectional switch rectifier operating under dual current control mode

Figure 5.11 (a) illustrates the three phase currents of the star-connected bidirectional switch boost rectifier over an entire fundamental cycle. Figure 5.11 (b) shows an expanded view of I_a. Three phase currents for the delta-connected bidirectional switch boost rectifier are shown in figure 5.12. From figures 5.11 and 5.12, it is apparent that the maximum peak-to-peak ripple in the line currents coincide with the theoretical limit set by equation (5.6).

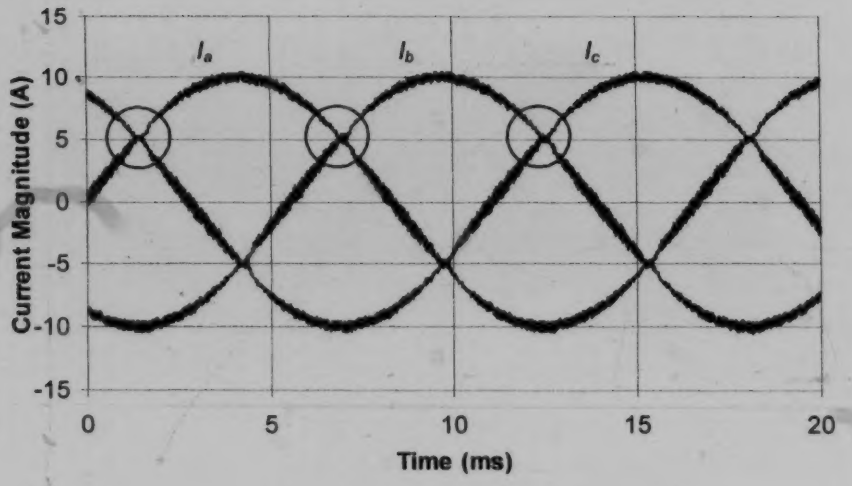


(a) Three phase line currents displayed over one fundamental cycle

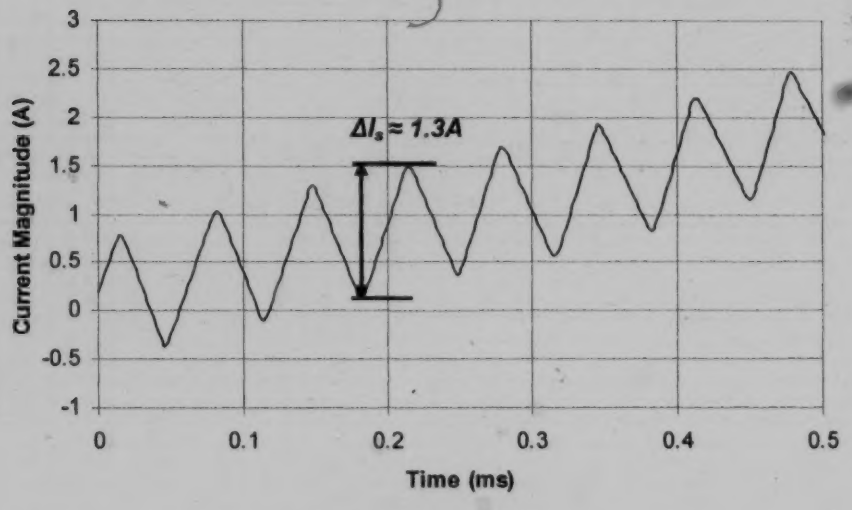


(b) Expanded view of I_a

Figure 5.11: Peak-to-peak current ripple for the star-connected bidirectional switch rectifier operating under dual current control mode



(a) Three phase line currents displayed over one fundamental cycle



(b) Expanded view of I_a

Figure 5.12: Peak-to-peak current ripple for the delta-connected bidirectional switch rectifier operating under dual current control mode

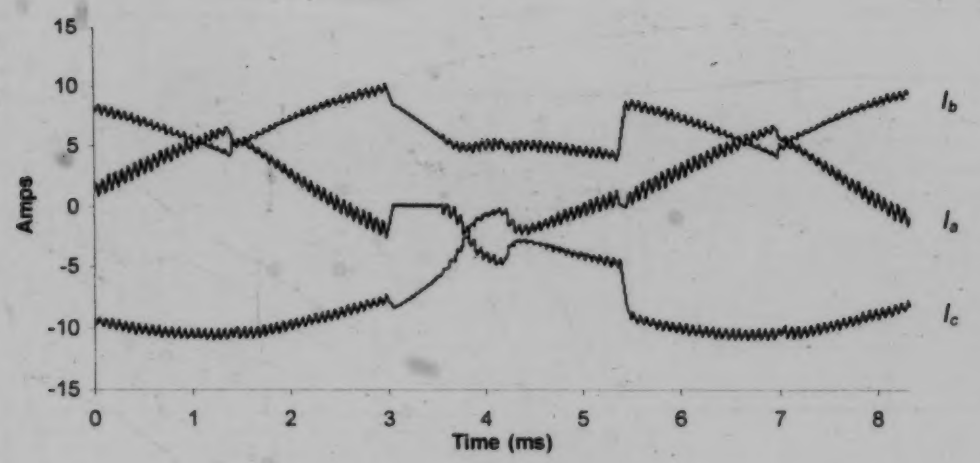
Compared to the stationary reference PI current controller and the proposed three phase current controller, 2-current control does not suffer from large high frequency distortions in the line currents (compare figures 5.2 (b) and 5.6 (b) with figures 5.11 (b) and 5.12 (b)). The stationary frame PI current controller and the proposed three phase

current controller are prone to high frequency distortions but the low frequency distortion is kept to a minimum. Conversely, the 2-current control scheme minimizes the high frequency distortion but low frequency distortions are present in the line currents (see figures 5.11 (a) and 5.12 (a)). These low frequency distortions occur whenever two phases cross each other (i.e. every 60°). During phase crossover, PWM for one of the phases sticks high (delta-connected configuration) or low (star-connected configuration) due to the nature of how the controller is designed, which leads to limited line-line voltage to force the phase current. As a result, the 2-current controller goes from controlling two currents to controlling one current during that time period leading to low frequency distortion.

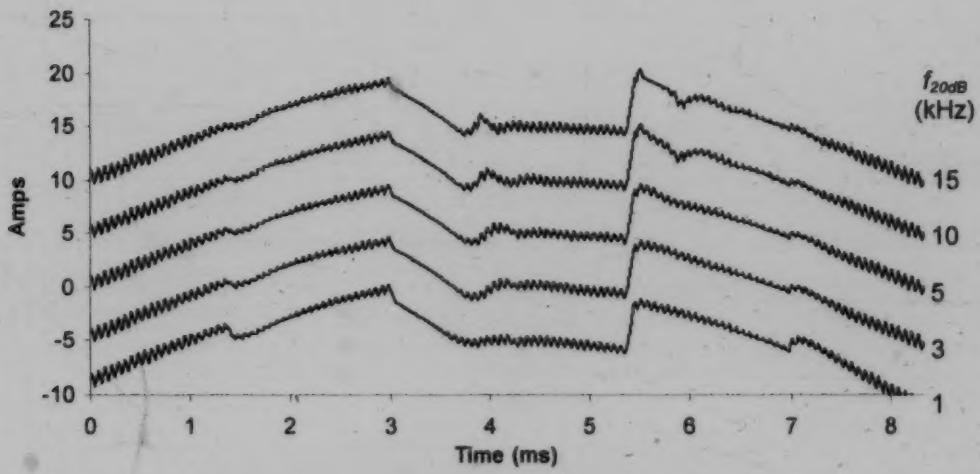
5.3.2 Transient Analysis and Effects of f_{20dB} on the Steady-State Current Errors

Transient analysis of the proposed 2-current control scheme is investigated using the procedure discussed in §5.1.2. Figure 5.13 (a) illustrates the effect of transient on the line current waveforms for a star-connected bidirectional switch boost rectifier; figure 5.13 (b) shows the effect of f_{20dB} on the transient response of the 2-current controller. Figure 5.14 (a) illustrates the effect of transient on the line current waveforms for a delta-connected bidirectional switch boost rectifier; figure 5.14 (b) shows the effect of f_{20dB} on the transient response of the 2-current controller.

Transient simulation results for the 2-current control scheme follow those of the proposed single and three phase current control techniques. The overshoots in the transient increase as the f_{20dB} frequency is increased. The low frequency distortion caused due to phase crossover decreases as the -20dB frequency is increased; however, the low frequency distortion caused by the current transient increases (see figures 5.13 (b) and 5.14 (b) at the 6 ms mark). Figures 5.13 and 5.14 suggest that 2-current control provides best performance at high f_{20dB} frequencies but is susceptible to current overshoots.

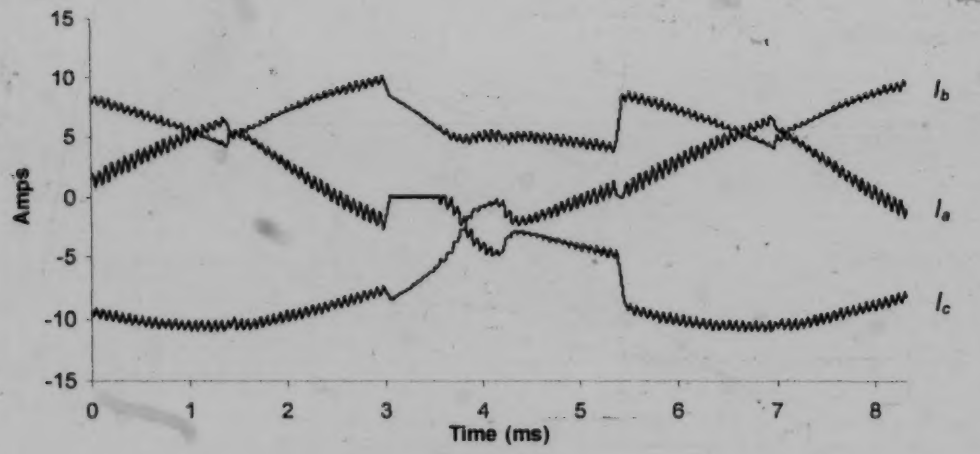


(a) Transient response showing all three phases (f_{20dB} = 1 kHz)

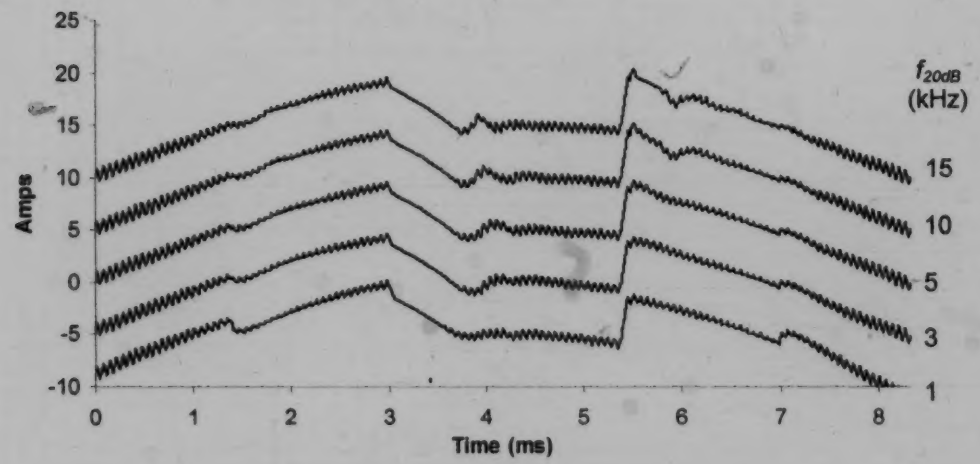


(b) Transient response of I_a for various f_{20dB} values

Figure 5.13: Offset waveforms: simulated transient response for the star-connected bidirectional switch rectifier operating under dual current control mode



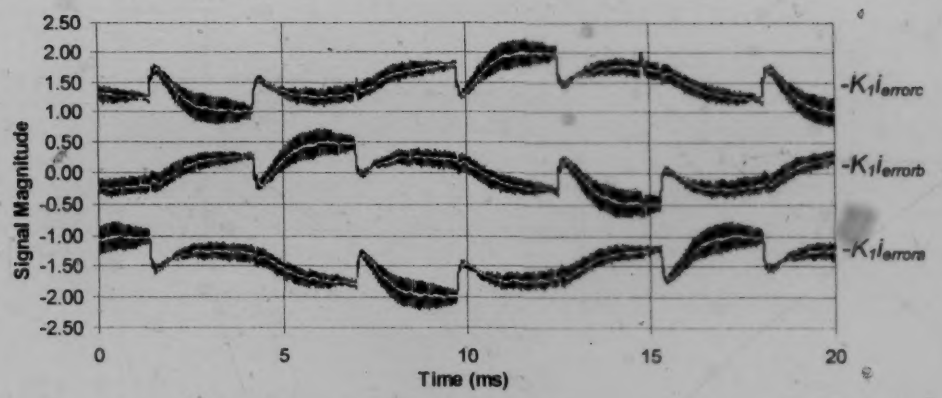
(a) Transient response showing all three phases (f_{20dB} = 1 kHz)



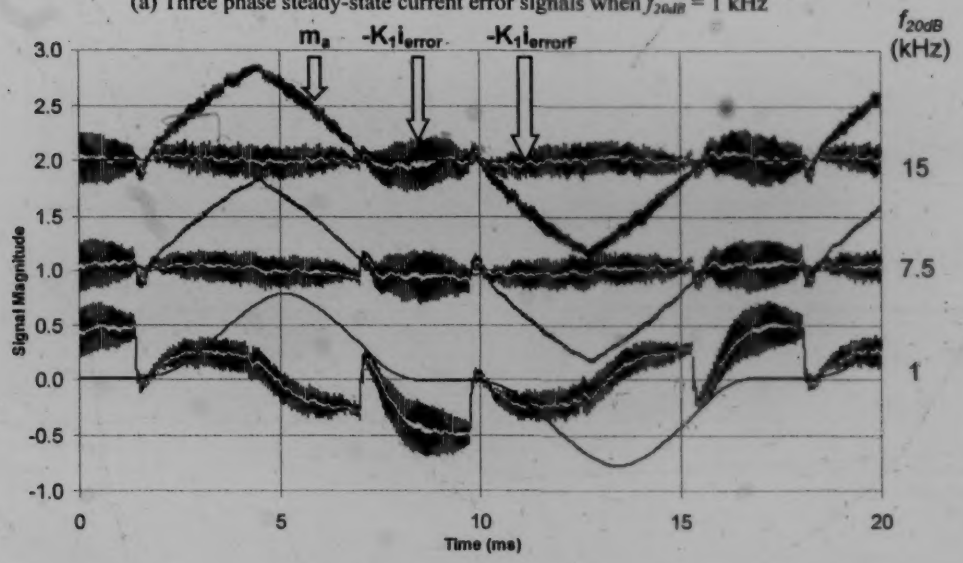
(b) Transient response of I_a for various f_{20dB} values

Figure 5.14: Offset waveforms: simulated transient response for the delta-connected bidirectional switch rectifier operating under dual current control mode

Figures 5.15 and 5.16 show the effect of f_{20dB} frequency on the steady-state current error signals for the star and delta-connected bidirectional switch boost rectifiers operating under the proposed dual current control mode.

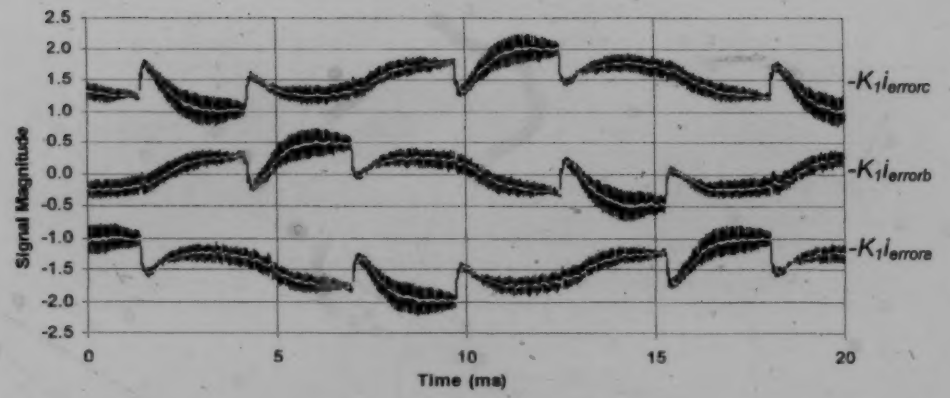


(a) Three phase steady-state current error signals when f_{20dB} = 1 kHz

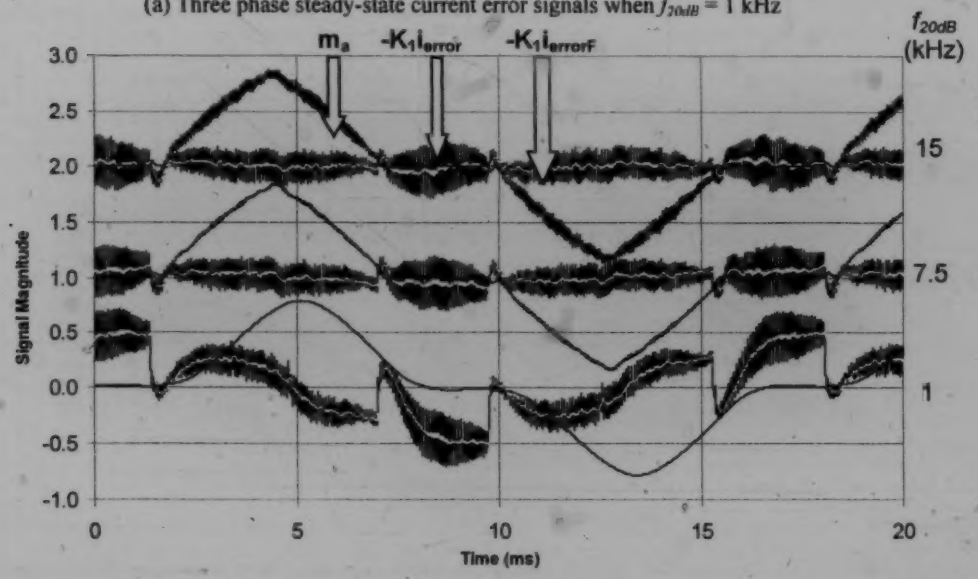


(b) Effect of f_{20dB} on $-K_1 i_{errora}$

Figure 5.15: Offset waveforms: effect of f_{20dB} on the steady-state current error for the star-connected bidirectional switch boost rectifier operating under dual current control mode



(a) Three phase steady-state current error signals when f_{20dB} = 1 kHz



(b) Effect of f_{20dB} on $-K_1 i_{errora}$

Figure 5.16: Offset waveforms: effect of f_{20dB} on the steady-state current error for the delta-connected bidirectional switch boost rectifier operating under dual current control mode

Figures 5.15 and 5.16 indicate that for low values of f_{20dB}, the steady-state current error signals for both configurations have a large fundamental component and the modulation depth signals have significant phase shift from their ideal cases; thus resulting in poor control performance.

5.4 Comparison of Three Phase Current Control Schemes Using Simulation Results

Comparison of the three phase current control techniques is presented through the investigation of their transient response and their ability to tolerate system disturbances. Each control scheme discussed in this chapter is tuned such as to provide a zero average steady-state current error in order to facilitate a comparison between them; typically, the current control schemes presented in this chapter provide a wide range of operation and control quality depending on how the controller is tuned. Figure 5.17 illustrates the steady-state current error signals during the current transient for the three phase current control schemes discussed above. Figure 5.18 shows the transient response of the various current control schemes.

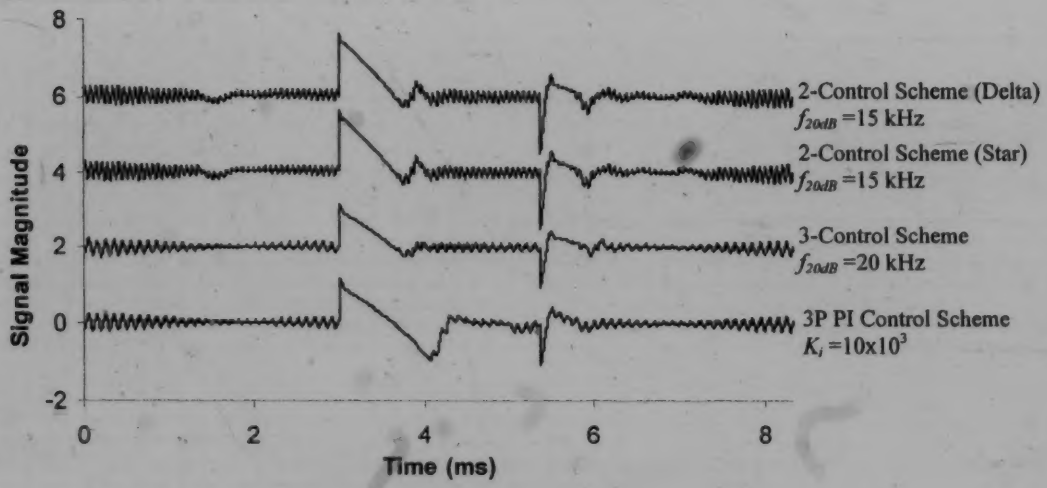


Figure 5.17: $-K_i i_{error}$ during a system transient

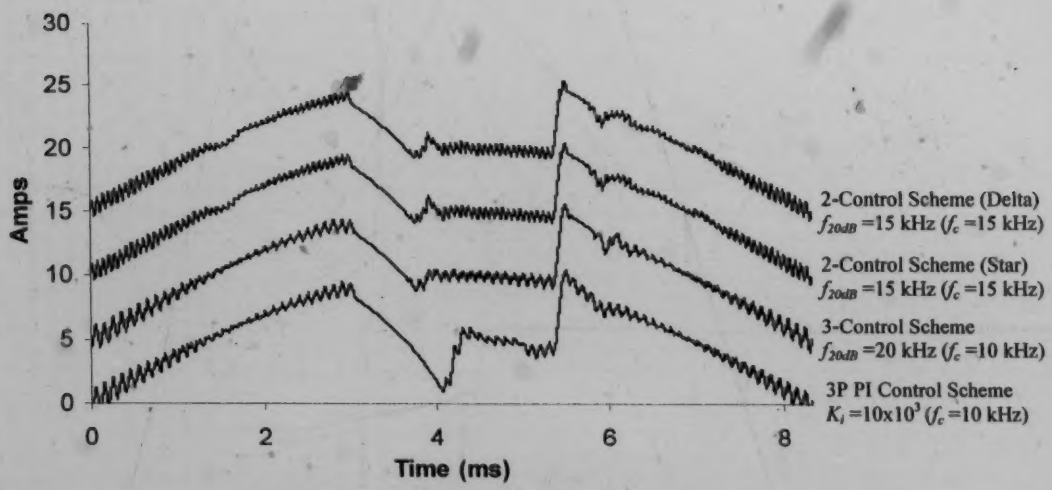
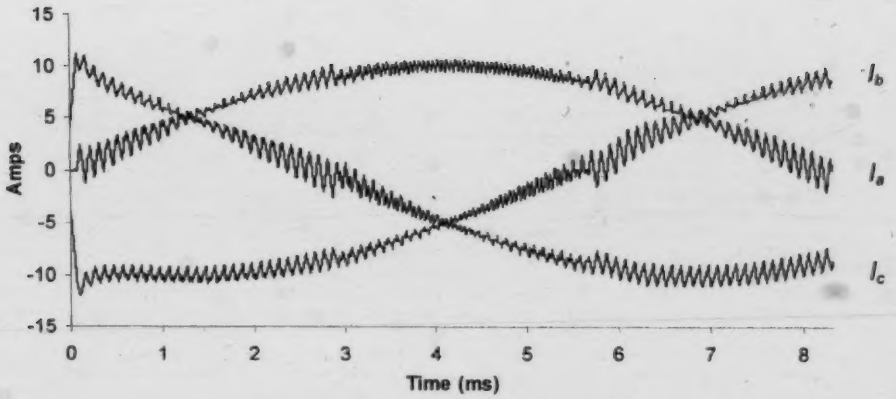


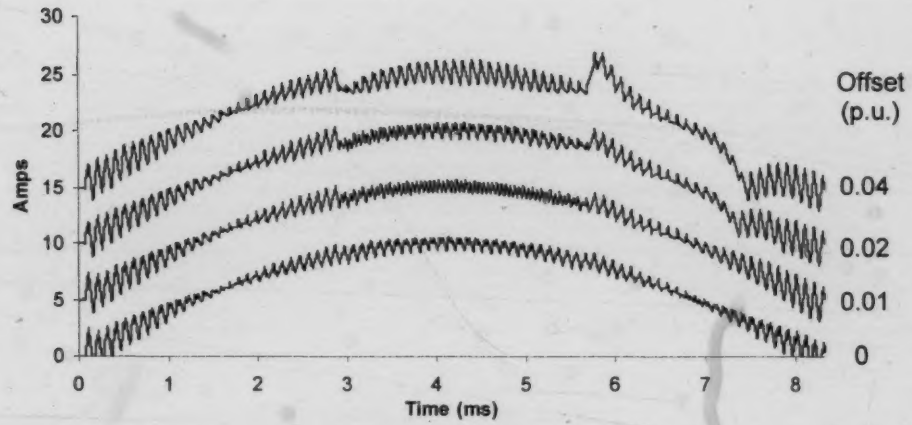
Figure 5.18: Three phase offset waveforms comparing the controller response to a step change in the demand current

The simulation results in figure 5.18 show that the proposed three phase current control and the propose 2-current control schemes have a more stable transient response with smaller current overshoots compared to the stationary frame PI current control scheme. The 3-current control scheme has a more damped response compared to the 2-current control schemes during the transient. Within the 2-current control schemes, a star-connected configuration yield are slightly more damped response to the step change than the delta-connected bidirectional switch boost rectifier.

In practical situations, a three phase system is never free of disturbances. Thus, the ability of a controller to tolerate small disturbances without loosing control displays the robustness of the scheme and is a highly desirable feature in the industry. By artificially introducing small offsets in the current reference signals, we can test the robustness of each controller to evaluate their tolerance to system disturbances and imperfections. The following figures shows the response of the various current control schemes to DC voltage offsets in the three current reference waveforms.

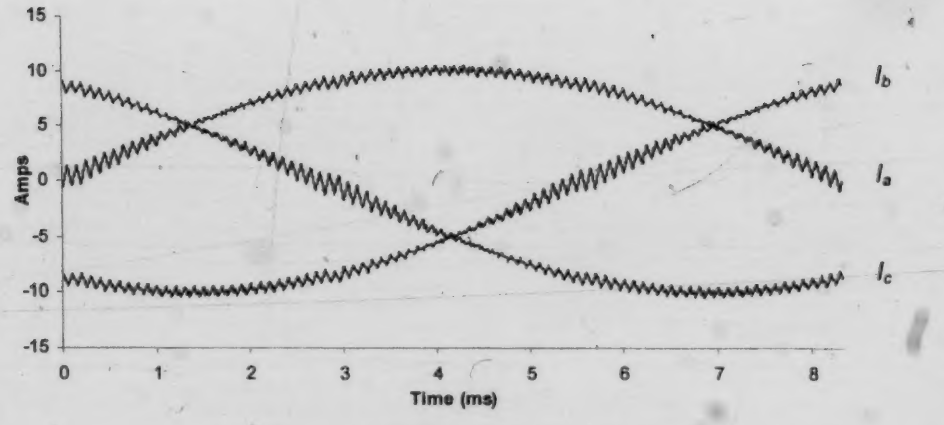


(a) 0.01 per-unit DC offset in i_{refc}, i_{refb}, and i_{refc}

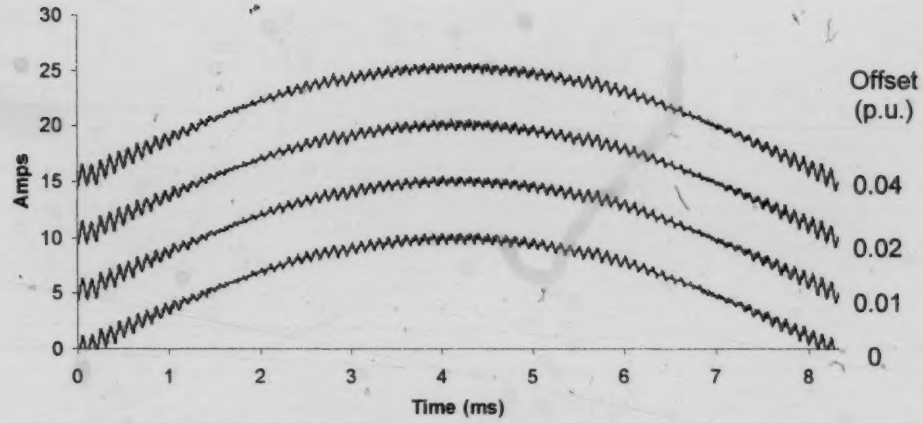


(b) Effect of DC offset on I_a

Figure 5.19: Offset waveforms: behaviour of stationary frame PI current control scheme under DC offset conditions

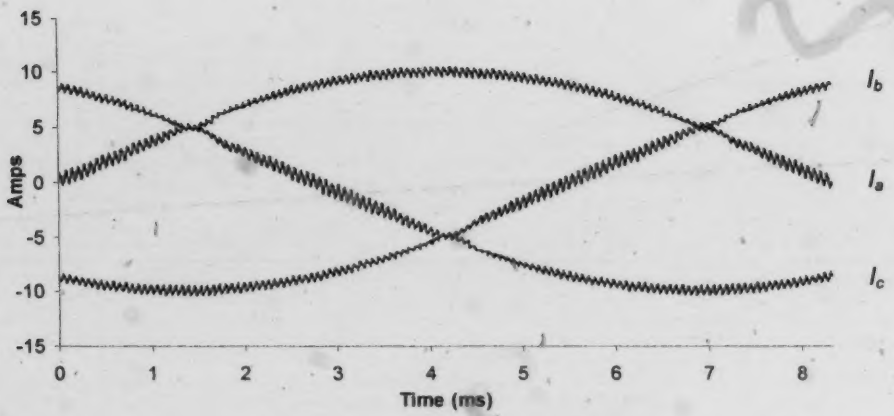


(a) 0.01 per-unit DC offset in i_{refc}, i_{refb}, and i_{refc}

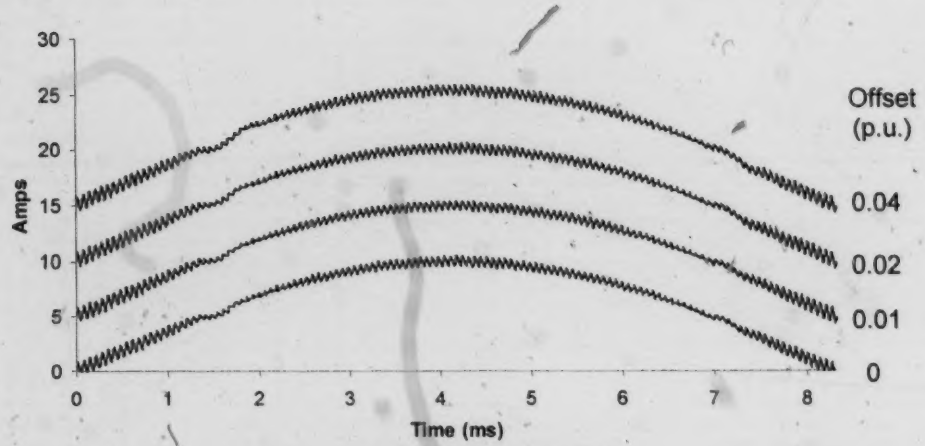


(b) Effect of DC offset in I_a

Figure 5.20: Offset waveforms: behaviour of the proposed three phase current control scheme under DC offset conditions

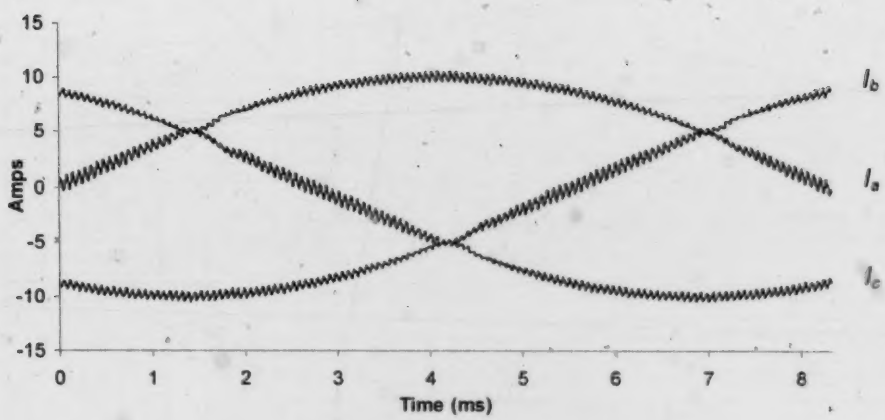


(a) 0.01 per-unit DC offset in i_{refc}, i_{refb}, and i_{refc}

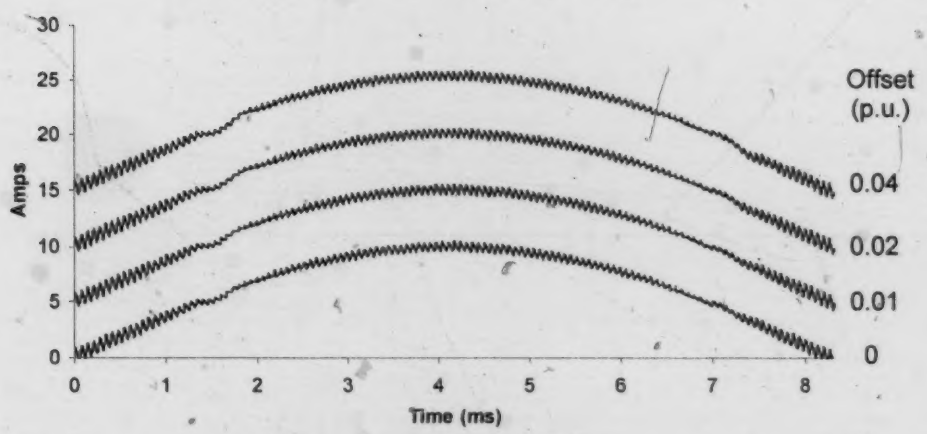


(b) Effect of DC offset on I_a

Figure 5.21: Offset waveforms: behaviour of the proposed 2- current control scheme under DC offset conditions (star-connected bidirectional switches)



(a) 0.01 per-unit DC offset in i_{refc}, i_{refb}, and i_{refc}



(b) Effect of DC offset on I_a

Figure 5.22: Offset waveforms: behaviour of the proposed 2- current control scheme under DC offset conditions (delta-connected bidirectional switches)

The proposed three phase current control and 2-current control techniques exhibit superior tolerance under DC voltage offset conditions compared to the stationary-frame PI current control scheme (compare figure 5.19 (b) with figures 5.20-5.22 (b)). Increasing the offset voltage in the current reference signals has negligible effect on the control performance of the proposed schemes. Conversely, increasing the offset voltage in the stationary frame PI current control scheme quickly leads to improper control and eventually instability of the control for high offset values (i.e. complete instability for values above 0.04 per-unit). Figure 5.22 illustrates that the proposed three phase current

control scheme is capable of tolerating DC offsets up to 0.1 per-unit in all three current reference signals before their performance matches that of the stationary frame PI current control scheme with 0.04 per-unit DC offset (compare figures 5.22 and 5.19 (a)).

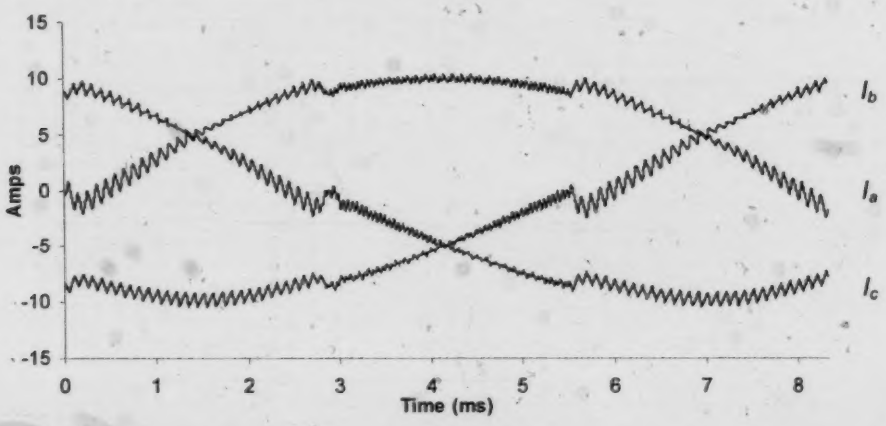
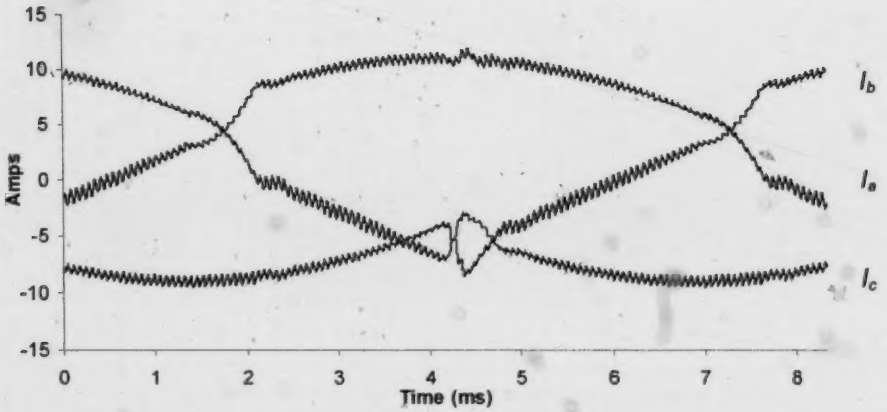
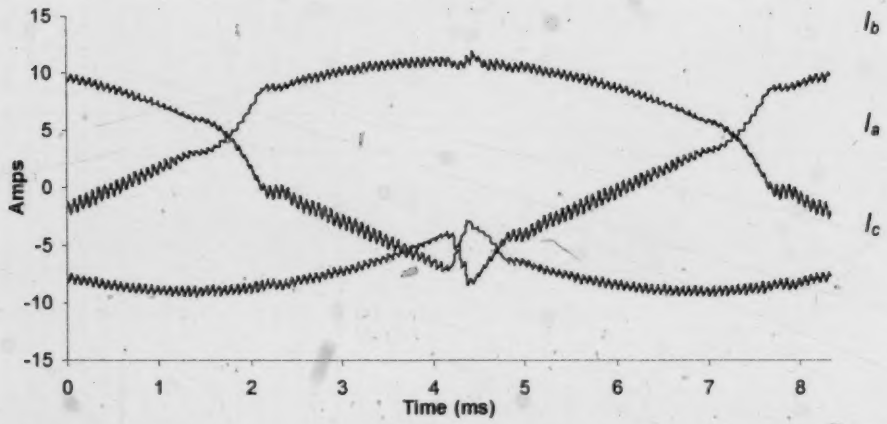


Figure 5.23: Behaviour of the proposed three phase current control scheme under 0.1 per-unit DC offset

Compared to the proposed three phase current control technique, the 2-current control technique shows a sharp decrease in the control quality and stability when a 0.1 per-unit DC offset is present in all three phases. This is primarily due to the nature of the switching pattern used in the dual current control mode. DC offsets introduce a phase shift in the current reference signals, which result in significant phase shifts in the modulation depth signal. In the dual current control mode, the switches are only switching 2/3rd of the overall switching period. Phase shifts in the current reference signal forces the voltage reference signals to be phase shifted into the region where the switching does not occur. This leads to missing switching pulses which deteriorates the line current waveforms.



(a) Star-connected bidirectional switch boost rectifier operating under dual current control mode



(b) Delta-connected bidirectional switch boost rectifier operating under dual current control mode

Figure 5.24: Behaviour of the 2-current control technique under 0.1 per-unit DC offset

5.5 Summary

Steady-state performance and the transient response of the stationary frame PI current control scheme and the proposed three phase current control and 2-current control techniques were tested using computer simulations. Furthermore, the behaviour of the current control schemes under system disturbances was also investigated. The proposed three phase current control technique and 2-current control technique yield stable steady-state operation, a quick transient response with minimal current overshoots, and an inherent tolerance to disturbances caused by phase interactions and DC offsets in the system when compared to a similarly tuned PI controller.

Chapter 6 Realization of the Current Control Schemes Using Analog Electronics

The proposed current control schemes are designed for implementation with readily available and low cost discrete electronic components. This chapter presents the design for analog circuitry used in the implementation of single and three phase current control schemes. Both single and three phase current controllers utilize similar analog circuitry due to the nature of their design. As such, circuitry designed for applications in the single phase current control schemes can be ported over to the three phase schemes using similar design procedures; alternative circuits are illustrated wherever the circuitry differs for single and three phase schemes. The voltage feedback signals are obtained using optocoupler-based voltage isolation equipment with a scaling ratio of 25:1; current feedback is obtained using LEM based current sensors. The design of the optocoupler-based voltage isolation equipment and the LEM current sensors are not discussed since it is beyond the scope of this thesis work and adds no further value to the proposed research other than providing the necessary feedback signals. The basic control diagram of the single phase PI current controller and the proposed single phase current control technique are illustrated in figures 4.1 and 3.5, respectively. The basic block diagram of the stationary reference frame PI current controller, the proposed three phase (3-current) current control scheme, and the 2-current control schemes are illustrated in figures 2.1, 3.6, and 3.10, respectively.

6.1 Generation of the Current Reference Template i_{ref}

In this section, the generation of a sinusoidal reference signal for the line current is discussed. Under ideal conditions, the current controller will force the line current to match the phase of i_{ref} while drawing sufficient current to satisfy the load demand. This circuit uses the feedback of the line voltage to generate a sinusoidal reference template for the line current (I_{sine}). Consider the circuit illustrated in the figure below.

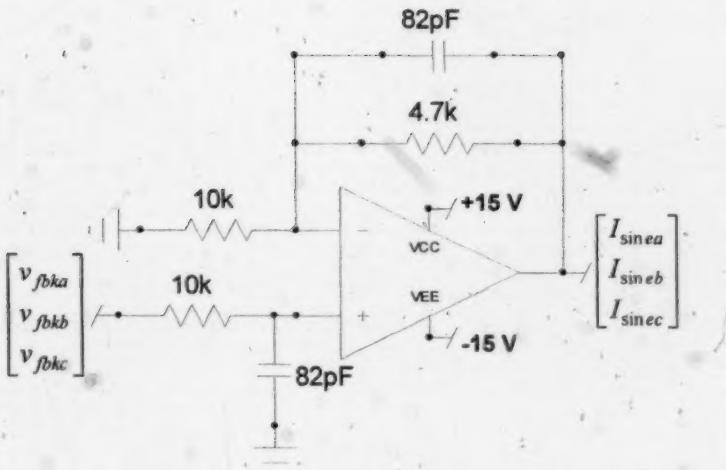


Figure 6.1: Sinusoidal Template Signal Generator

Considering only phase "a", the voltage feedback is obtained by using optocoupler based voltage isolation equipment. With a scaling ratio of 25:1, which implies that if the phase voltage is 120 V_{RMS} (or 169.7 V_{pk}), the isolated signal applied to the input of this circuit will be 4.8 V_{RMS} (or approximately 6.79 V_{pk}). This configuration utilizes a single op-amp differential amplifier stage, with capacitors added for high frequency noise filtering, and has an overall voltage gain of 1.47 V/V so that the magnitude of the output signal is approximately 10 V_{pk}.

For single phase applications, only one such circuit is required as there is only one line voltage. For three phase applications, three separate sinusoidal template signal generators are used, one for each phase voltage (I_{sinea}, I_{sineb}, I_{sinec}). This allows for the generation of three independent sinusoidal template signals which then can be used to generate the current reference signals i_{refa}, i_{refb}, i_{refc}.

For closed loop operation, the controller should be able to fix the output voltage of the PWM rectifier to some reference value set by the user. In order to do this, the controller must be capable of adjusting the magnitude of the demand current, and consequently the supply current, to provide the desired output DC voltage. By utilizing the error between the desired output voltage and the scaled DC link voltage feedback

signal, one can generate a signal I_{mag} that automatically adjusts the magnitude of the line currents via their respective current reference signals. Figure 6.2 illustrates the circuits utilized to obtain the magnitude of the current demand signal.

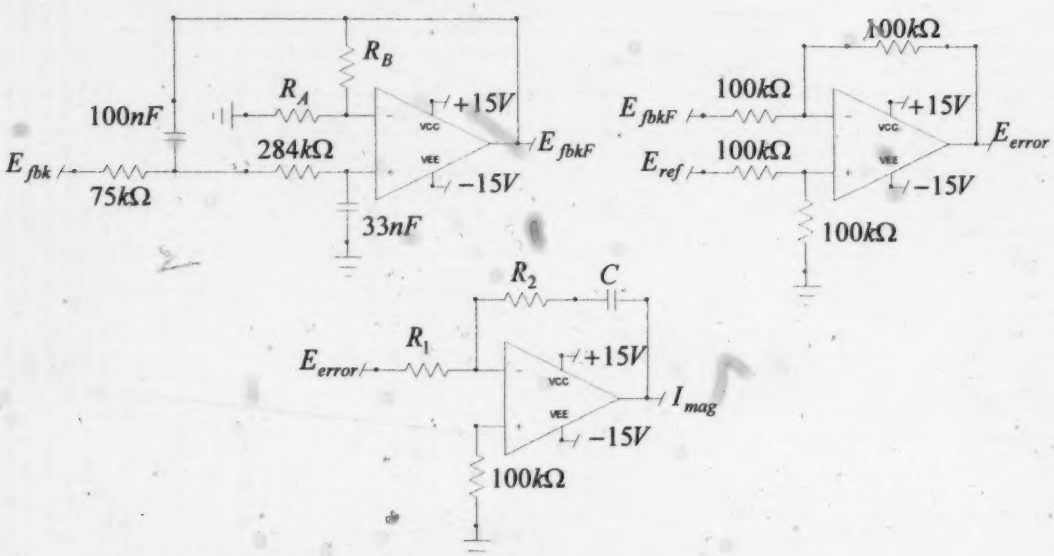


Figure 6.2: Current demand signal generation

The DC link feedback voltage is passed through a low pass second order Butterworth filter with an f_{20dB} frequency equal to 60 Hz. The -20dB attenuation frequency is the frequency at which the output signal magnitude is $1/10^{th}$ of the input signal magnitude ($f_{20dB} \approx 3.14 \times f_{3dB}$). For the single phase current control schemes, the gain of the filter need to be designed such that for a 200 V DC link voltage, we obtain a 10 V signal on the filter output. The filter gain for a low pass 2^{nd} order Butterworth filter is given by:

$$K = 1 + \frac{R_B}{R_A} \qquad (6.1)$$

Using the optocoupler based voltage isolation equipment discussed previously, the DC link voltage feedback signal and the respective filter gain for the single phase current control schemes are given by the following expressions.

$$E_{fbk\ 1P} = \frac{200V}{25} = 8V \tag{6.2}$$

$$K_{f\ 1P} = \frac{10V}{8V} = 1.25 \tag{6.3}$$

From equations (6.1) and (6.3), resistors R_A and R_B can be calculated to give the required filter gain.

$$K_{f\ 1P} = 1.25 = 1 + \frac{R_B}{R_A} \Rightarrow R_B = 0.25 \times R_A \tag{6.4}$$

Let $R_A = 100k\Omega \Rightarrow R_B = 25k\Omega$ **(6.5)**

Note that similar results can be obtained for three phase control schemes as well.

$$E_{fbk\ 3P} = \frac{300V}{25} = 12V \tag{6.6}$$

For the sake of simplicity, the DC link feedback signal for three phase current control schemes is attenuated using a voltage divider network such that the three phase filter gain is equal to the single phase filter gain (i.e. $E_{fbk\ 3P} = 8V$, $K_{f\ 3P} = 1.25$). This allows us to use the same filter design as used in the single phase current control schemes.

The output of the filter is compared with a DC reference signal to generate the DC link voltage error signal, which is then passed through a PI compensator to generate I_{mag}. The transfer function of a PI compensator shown in figure 6.2 is given by equation (6.6).

$$T(s) = -\left(K_p + \frac{K_i}{s}\right) \tag{6.7}$$

For single phase control schemes, f_c = 5 kHz, L_s = 5 mH, V_{DC} = 200V:

$$K_p = \frac{R_2}{R_1} = 10 \times K_1 = 10\left(\frac{4 f_c L_s}{E}\right) = 10\left(\frac{4 \times 5kHz \times 5mH}{200V}\right) = 5 \tag{6.8}$$

$$R_2 = 5 \times R_1 \rightarrow Let\ \underline{R_1 = 100k\Omega} \Rightarrow \underline{R_2 = 500k\Omega} \tag{6.9}$$

$$K_i = \frac{1}{R_1 C} = 4 f_s \Rightarrow C = \frac{1}{100k\Omega\ (4 \times 60Hz)} = 41.7nF \approx \underline{42nF} \tag{6.10}$$

For three phase control schemes, f_c = 10 kHz, L_s = 2.5 mH, V_{DC} = 300V:

$$K_p = \frac{R_2}{R_1} = 10 \times K_1 = 10\left(\frac{3 f_c L_s}{E}\right) = 10\left(\frac{3 \times 10kHz \times 2.5mH}{300V}\right) = 2.5 \tag{6.11}$$

$$R_2 = 2.5 \times R_1 \rightarrow Let\ \underline{R_1 = 100k\Omega} \Rightarrow \underline{R_2 = 250k\Omega} \tag{6.12}$$

$$K_i = \frac{1}{R_1 C} = 4 f_s \Rightarrow C = \frac{1}{100k\Omega\ (4 \times 60Hz)} = 41.7nF \approx \underline{42nF} \tag{6.13}$$

I_{sine} provides the sinusoidal phase template for the current reference signal; I_{mag} represents the peak magnitude of the current reference signal. Using I_{sine} and I_{mag}, the current reference signal can be obtained as follows:

$$i_{ref\,n} = I_{\sin e\,n} \times I_{mag} \quad where \quad n = a,b,c \tag{6.14}$$

6.2 Generation of the Current Feedback Signal (i_{fbk})

In this section, generation of the current feedback signal is discussed. The output from the LEM current sensors yields a current to voltage ratio of 1A = 0.5V. Figure 6.3 shows the basic circuit used to obtain the current feedback signal.

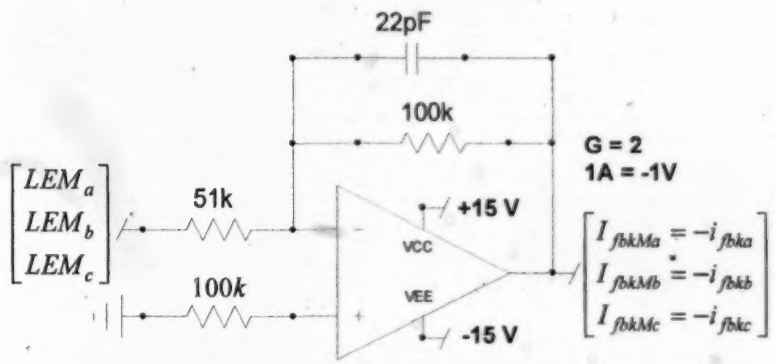


Figure 6.3: Current feedback signal i_{fbk}

The output of the LEM current sensor is passed through an inverting amplifier with high frequency noise filtering. The resulting signal is equal to the line current in magnitude but inverted in phase; this phase inversion simplifies the generation of the current error signal in the later design stages. Single phase current control schemes only require one such circuit since only one LEM is required to feedback the line current; for three phase applications, three LEM current sensors are used (one for each phase) and as

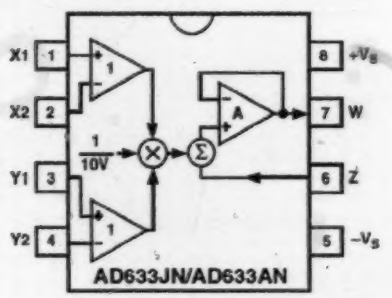
such, require the use of three independent circuits to generate the line current feedback signals.

6.3 Generation of the Current Error Signal (i_{error})

The current error signal is crucial to the operation of the single and three phase current control schemes studied in this thesis work. The current error signal (i_{error}) represents the difference between the actual line current (i_{fbk}) and the desired current value (i_{ref}). i_{ref} is obtained by multiplying I_{sine} with I_{mag} using an AD633 analog multiplier IC. Generation of the three phase current error signals can be expressed as follows:

$$\begin{bmatrix} i_{errora} \\ i_{errorc} \\ i_{errorc} \end{bmatrix} = \begin{bmatrix} i_{refa} \\ i_{refb} \\ i_{refc} \end{bmatrix} - \begin{bmatrix} i_{fbka} \\ i_{fbkb} \\ i_{fbkc} \end{bmatrix} = I_{mag} \times \begin{bmatrix} I_{sinea} \\ I_{sineb} \\ I_{sinec} \end{bmatrix} + \begin{bmatrix} i_{fbkMa} \\ i_{fbkMb} \\ i_{fbkMc} \end{bmatrix} \tag{6.15}$$

Along with the ability to multiply two signals, the AD633 also has the ability to add two signals. The transfer function of the AD633 analog multiplier IC is given by the following figure.



$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z$$

Figure 6.4: Block diagram and transfer function of AD633 analog multiplier

The inverted current feedback signal (i_{fbkM}) can be utilized to obtain the current error signal by adding it with i_{ref} as illustrated by equation (6.15). This is equivalent to subtracting the actual line current (i_{fbk}) from the desired current value which consequently results in the current error signal. The expression for the current error signal for phase "a" can be expressed as follows:

$$i_{errora} = \frac{(I_{mag} - 0)(I_{sinea} - 0)}{10V} + (-i_{fbka}) = \frac{I_{mag} \times I_{sinea}}{10V} + i_{fbkMa} \tag{6.16}$$

Figure 6.5 shows the basic circuitry used to generate the current error signals. For single phase applications, only one analog multiplier is required; for three phase control schemes, three analog multiplier ICs are utilized to generate the current error signal for each line current.

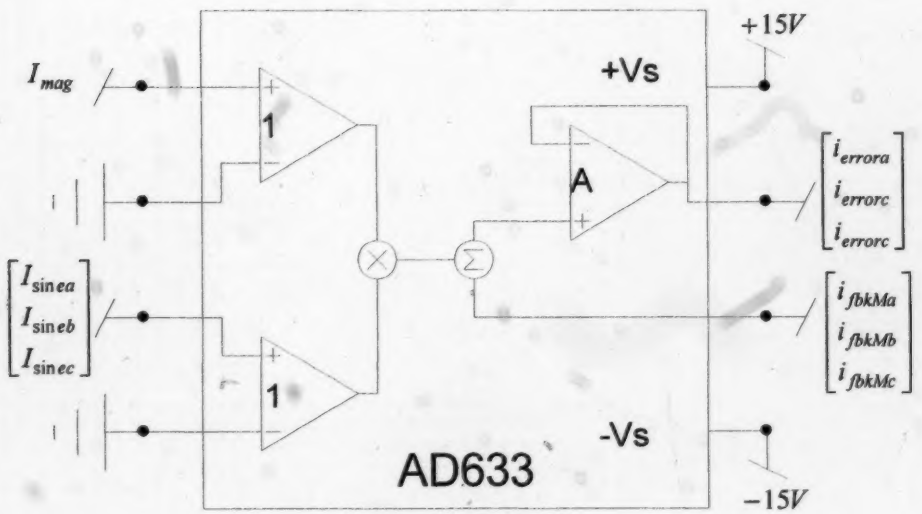


Figure 6.5: Current error signal generation

6.4 Generation of the Voltage Reference Signal (v_{ref})

The input voltage reference signal of the PWM generator can be obtained by either using PI compensator(s) or by adding the modulation depth signal(s) with the scaled current error signal(s) depending on which current control scheme is being utilized. The circuits remain unchanged regardless of whether the controller is single phase or three phase in nature.

6.4.1 Design of a PI Compensator

The transfer function of the PI compensator used in the generation of the voltage reference signal for PWM modulation is given by:

$$T(s) = -\left(K_p + \frac{K_i}{s}\right) \Rightarrow v_{ref}(s) = -\left(K_p i_{error\ n}(s) + \frac{K_i i_{error\ n}(s)}{s}\right) \tag{6.17}$$

where $n = a, b, c$

From equation (6.17), the integral gain K_i improves the tracking by minimizing the instantaneous error between the current reference signal and the actual current; the proportional gain term K_p affects the overall current ripple and consequently the maximum peak-to-peak ripple of the current error signal. Figure 6.6, illustrates a basic analog representation of a PI compensator typically used in the industry for current control applications.

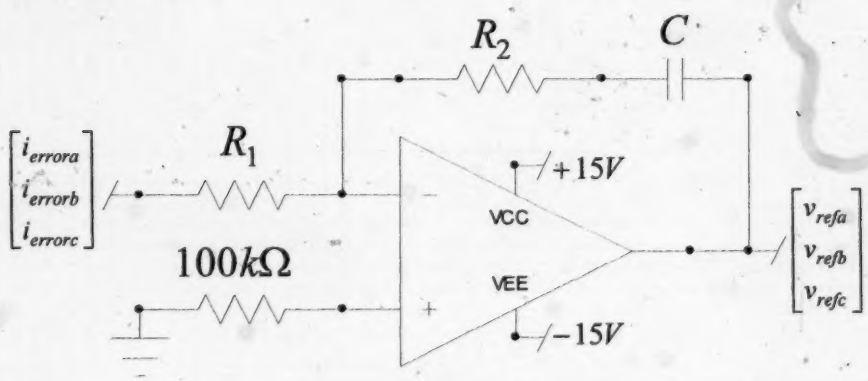


Figure 6.6: PI compensator

In order to reduce the influence of noise on the analog circuitry, the per-unit signals from the simulations are converted to more practical signals using a base magnitude of 10V. The proportional and integral gain terms are calculated as follows:

$$K_p = \frac{R_2}{R_1} = 10 \times K_1 \tag{6.18}$$

$$K_i = \frac{1}{R_1 C} = f_c \tag{6.19}$$

For the single phase PI current control scheme, f_c = 5 kHz, L_s = 5 mH, V_{DC} = 200V:

$$K_p = \frac{R_2}{R_1} = 10 \times K_1 = 10\left(\frac{4 f_c L_s}{V_{DC}}\right) = 10\left(\frac{4 \times 5kHz \times 5mH}{200V}\right) = 5 \tag{6.20}$$

$$R_2 = 5 \times R_1 \rightarrow Let\ \underline{R_1 = 100k\Omega} \Rightarrow \underline{R_2 = 500k\Omega} \quad (6.21)$$

$$K_i = \frac{1}{R_1 C} = f_c \Rightarrow C = \frac{1}{100k\Omega\ (5kHz)} = \underline{2nF} \quad (6.22)$$

For the three phase stationary reference frame PI current control scheme, f_c = 10 kHz, L_s = 2.5 mH, V_{DC} = 300V:

$$K_p = \frac{R_2}{R_1} = 10 \times K_1 = 10\left(\frac{3 f_c L_s}{V_{DC}}\right) = 10\left(\frac{3 \times 10kHz \times 2.5mH}{300V}\right) = 2.5 \quad (6.23)$$

$$R_2 = 2.5 \times R_1 \rightarrow Let\ \underline{R_1 = 100k\Omega} \Rightarrow \underline{R_2 = 250k\Omega} \quad (6.24)$$

$$K_i = \frac{1}{R_1 C} = f_c \Rightarrow C = \frac{1}{100k\Omega\ (10kHz)} = \underline{1nF} \quad (6.25)$$

6.4.2 Generating v_{ref} for the Proposed Current Control Schemes (3-Current and 2-Current Control Modes)

In the proposed current control schemes, the voltage reference signal for the PWM signal can be generated by taking the difference between the modulation depth signal and the respective current error signal. Figure 6.7 illustrates a differential amplifier used for obtaining the voltage reference signal(s) for PWM modulation.

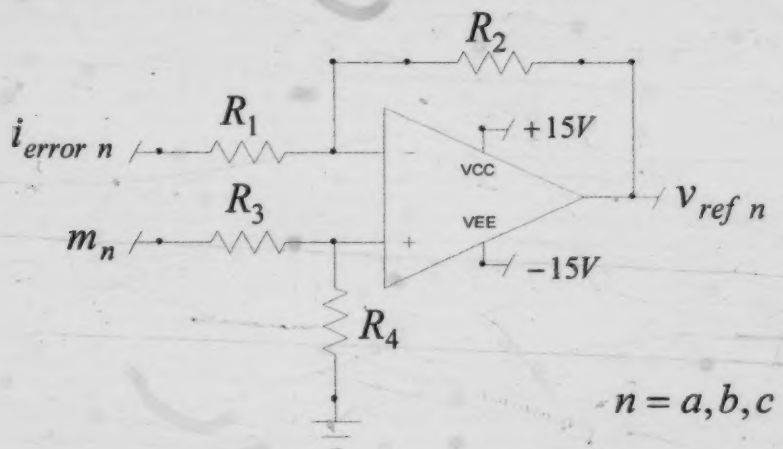


Figure 6.7: Generating v_{ref} using the modulation depth signal

The resistor values in figure 6.7 need be calculated such that the voltage reference signal is given by the following expression:

$$v_{ref\,n} = m_n - K_p i_{error\,n}, \quad where \quad K_p = 10 \times K_1 \tag{6.26}$$

Using the Superposition Theorem:

$$-K_p i_{error\,n} = -i_{error\,n} \frac{R_2}{R_1} \Rightarrow R_2 = K_p R_1 \tag{6.27}$$

$$m_n = m_n \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_1} \right) = m_n \left(\frac{R_4}{R_3 + R_4} \right) \left(\frac{R_1 + K_p R_1}{R_1} \right) \tag{6.28}$$

Simplifying equation (6.28):

$$1 = \left(\frac{R_4}{R_3 + R_4} \right) \left(K_p + 1 \right) \Rightarrow R_4 = \frac{R_3}{K_p} \tag{6.29}$$

For the proposed single phase current control technique, K_p = 5:

$$\begin{aligned} &Let \quad \underline{R_1 = 100k\Omega} \Rightarrow \underline{R_2 = 500k\Omega} \\ &Let \quad \underline{R_3 = 100k\Omega} \Rightarrow \underline{R_4 = 20k\Omega} \end{aligned} \tag{6.30}$$

For the proposed three phase and 2-current control techniques, K_p = 2.5:

$$\begin{aligned} &Let \quad \underline{R_1 = 100k\Omega} \Rightarrow \underline{R_2 = 250k\Omega} \\ &Let \quad \underline{R_3 = 100k\Omega} \Rightarrow \underline{R_4 = 40k\Omega} \end{aligned} \tag{6.31}$$

6.5 Generation of the Triangle Carrier Signals

In Chapters 4 and 5, the carrier signals used in the simulation results were generated functionally without the use of discrete components. Single phase current control techniques required the use of a carrier signal which ramped between ±1V due to the per-unit nature of the current error and the voltage reference signals. Three phase current control schemes utilized PD PWM modulation with two carriers, ramping between 0 to 1V and 0 to -1V, arranged such that the phase difference between them is zero (see figure 3.16). The subsequent subsections present the design of the triangle wave carrier signals for single and three phase PWM modulation using discrete analog components.

6.5.1 Carrier Signal for Single Phase Current Control Schemes

The resultant v_{ref} signals from §6.3 have a signal magnitude of ±10V peak. To prevent over-modulation of the PWM signals and minimize the influence of noise on the analog circuitry, the carrier signal magnitude is amplified to ±10V peak. Figure 6.8 illustrates the analog circuitry used for generating the voltage signal for the single phase current control techniques. The carrier frequency can be varied simply by changing the capacitance C in the circuit.

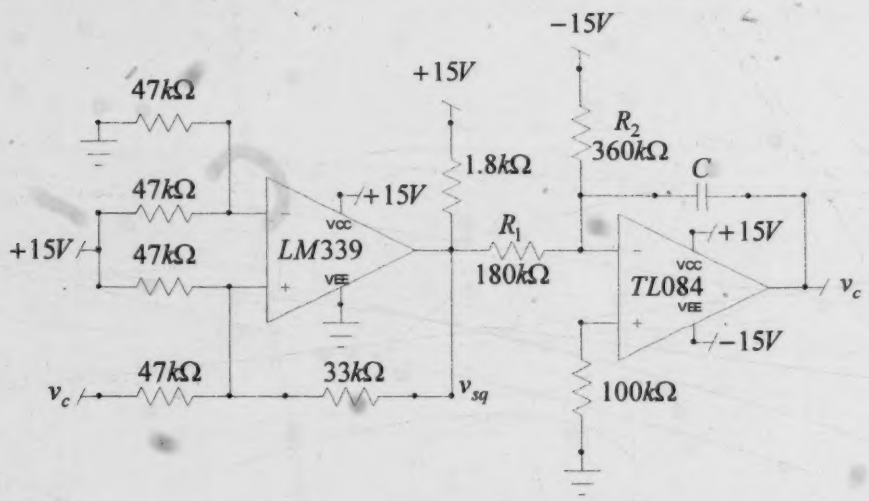


Figure 6.8: Analog carrier signal generator: ± 10V peak

This circuit uses the feedback of the carrier signal to create a closed loop self-oscillating system. The comparator circuit (LM339) converts the analog carrier signal into a digital output (v_{sq}); v_{sq} is then integrated using an integral circuit (TL084) to generate the carrier signal. The transfer function of the integrator circuit is given by:

$$\left|\frac{dv_c}{dt}\right| = \frac{v_{sq}}{R_1 C} + \frac{|-15V|}{R_2 C} \qquad \textbf{(6.32)}$$

If the carrier frequency is f_c and the peak signal magnitude is ±10V, the input signal v_{sq} has the same frequency and pulses between 0 and +15V.

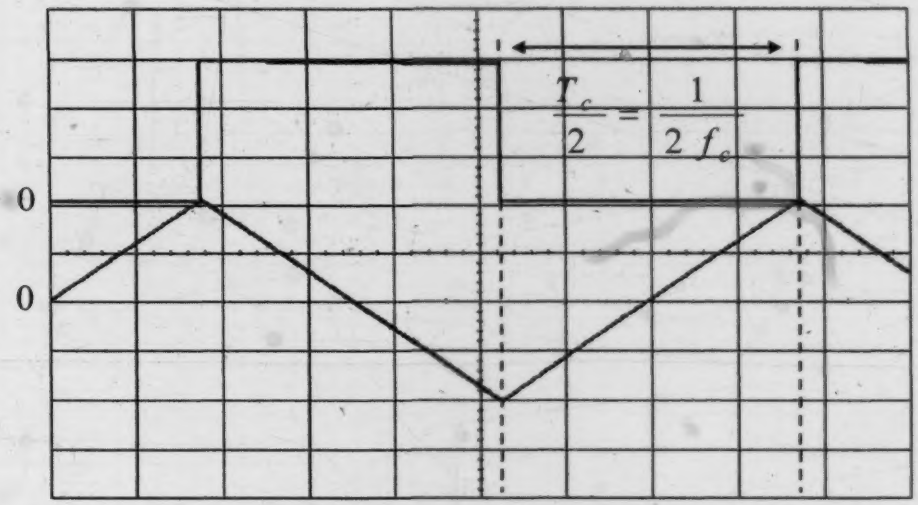


Figure 6.9: v_{sq} and v_c: 5V/div

From figure 6.9, during the time period $\frac{T_c}{2} = \frac{1}{2f_c}$, the magnitude of the square wave is 0V and the carrier signal varies from -10V to +10V. Thus, equation (6.32) can be simplified as followed:

$$\left|\frac{-10V-(+10V)}{1/2f_c}\right| = \frac{0}{R_1C} + \frac{15V}{R_2C} \Rightarrow \frac{20}{15} = \frac{1}{2f_cR_2C} \qquad \textbf{(6.33)}$$

Letting $R_2 = 2R_1$, the required capacitance is given by:

$$C = \frac{15}{20} \times \frac{1}{4R_1f_c} \qquad \textbf{(6.34)}$$

For $R_1 = 180\text{k}\Omega$ and varying switching frequencies, the required capacitance is:

$$C = \frac{15}{20} \times \frac{1}{4R_1f_c} = \frac{15}{20} \times \frac{1}{4(180k\Omega)f_c}$$

$$For \quad f_c = 5kHz \Rightarrow C = 0.208nF \approx 0.2nF$$

$$For \quad f_c = 10kHz \Rightarrow C = 0.104nF \approx 0.1nF$$

$$For \quad f_c = 15kHz \Rightarrow C = 69.4pF \approx 69pF$$

6.5.2 Carrier Signals for Three Phase Current Control Techniques

The carrier signal developed in subsection 6.5.1 is modified in order to generate the two carrier signals necessary for phase disposition PWM modulation. Mathematically, the upper (v_{cp}) and lower (v_{cn}) carrier signals can be obtained by the following expressions:

$$v_{cp} = \frac{v_c}{2} + 5V \tag{6.35}$$

$$v_{cn} = v_{cp} - 10V \tag{6.36}$$

Analog representation of equations (6.35) is illustrated in figure 6.10.

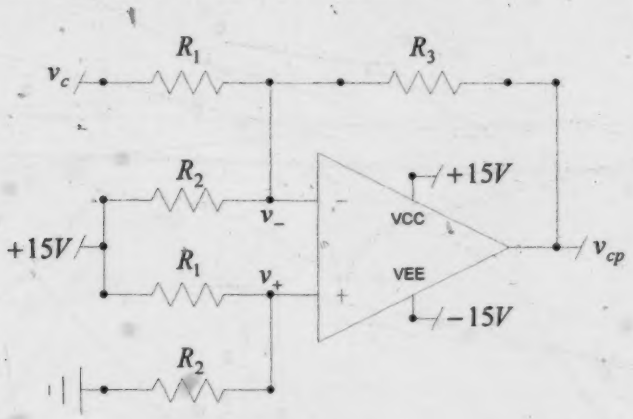


Figure 6.10: v_{cp} generation: 0V to +10V

In order to attenuate the v_c by half (i.e. from ±10V to ±5V):

$$\frac{R_3}{R_1} = \frac{5}{10} \Rightarrow R_3 = \frac{R_1}{2} \tag{6.37}$$

The ratio of resistor values necessary for providing a +5V DC bias on the $v_c/2$ signal can be expressed as follows:

$$v_+ = v_- = 5V = \frac{R_1}{R_1 + R_2}(15V) \Rightarrow R_2 = 2R_1 \tag{6.38}$$

Using equations (6.37) and (6.38):

$$Let \quad \underline{R_1 = 10k\Omega} \Rightarrow \underline{R_2 = 20k\Omega}, \quad \underline{R_3 = 5k\Omega} \tag{6.39}$$

Figure 6.11 shows the analog circuit used to generate the lower carrier signal for three phase current control techniques.

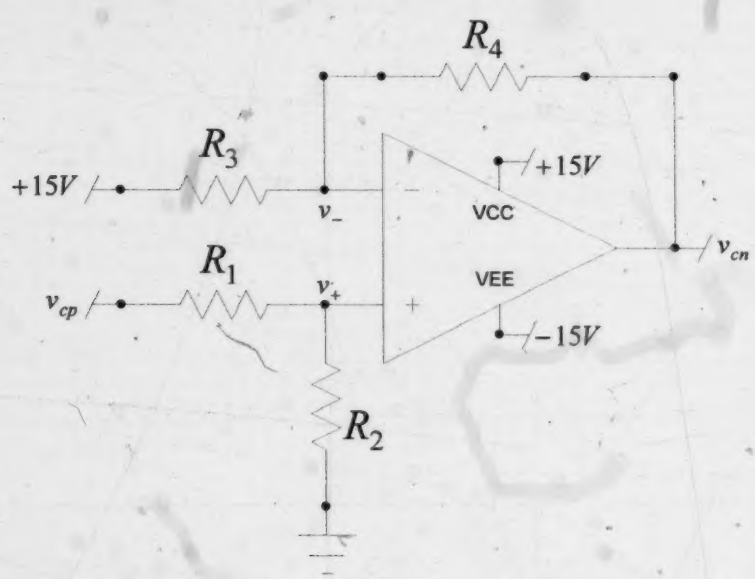


Figure 6.11: v_{cn} generation: 0V to -10V

From figure 6.11 and equation (6.36), v_{cn} can be expressed as follows:

$$v_{cn} = v_{cp}\frac{R_2}{R_1+R_2}\left(\frac{R_3+R_4}{R_4}\right)-(+15V)\frac{R_4}{R_3} = v_{cp} - 10V \qquad \textbf{(6.40)}$$

Using law of superposition on equation (6.40) yields:

$$10V = (+15V)\frac{R_4}{R_3} \Rightarrow R_3 = \frac{3}{2}R_4 \qquad \textbf{(6.41)}$$

$$v_{cn} = v_{cp}\frac{R_2}{R_1+R_2}\left(\frac{R_3+R_4}{R_4}\right) = v_{cp}\frac{R_2}{R_1+R_2}\left(\frac{\frac{3}{2}R_4+R_4}{\frac{3}{2}R_4}\right) \Rightarrow R_2 = \frac{3}{2}R_1 \qquad \textbf{(6.42)}$$

Using equations (6.41) and (6.42):

$$\textit{Let}\quad \underline{R_1 = R_4 = 10k\Omega}, \Rightarrow \underline{R_2 = 15k\Omega},\ \underline{R_3 = 15k\Omega} \qquad \textbf{(6.43)}$$

Figure 6.12 shows the upper and lower carrier signals generated by the circuits illustrated in figures 6.10 and 6.11.

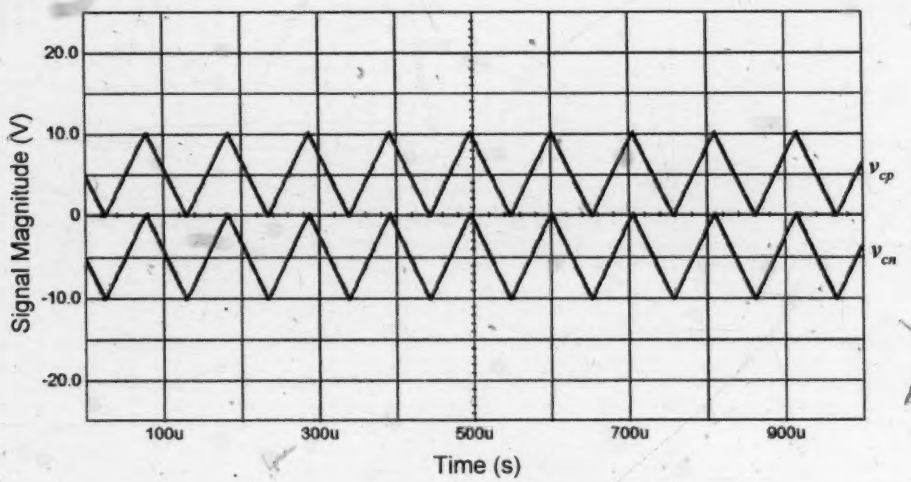


Figure 6.12: v_{cp} and v_{cn} signal waveform

6.6 PWM Signal Generator for the Single Phase Current Control Techniques

The pulse width modulation signals are generated by comparing the voltage reference signal(s) with the carrier signal. Switching occurs when ever there is an intersection between the carrier signal and the reference signal. Figure 6.13 shows the PWM signal generator for the single phase current control schemes.

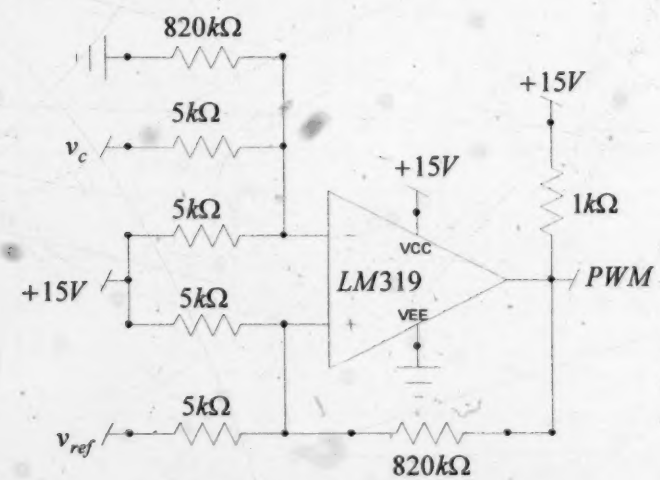
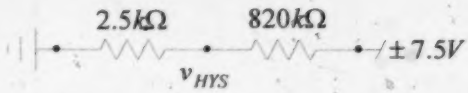


Figure 6.13: Single phase PWM signal generator

When looking at the output, the PWM signal varies between 0.1V and 14.9V (i.e. ±7.4V).



The voltage signal present at node v_{HYS} is 22.5mV. However, the input signal is attenuated 50% by the input resistors. Therefore, the effective hysteresis is doubled to a value of 45mV.

The actual switching signal S applied to the single phase PWM boost rectifier can be obtained by the using the following circuits. However, before the PWM signal is fed into the logic circuitry, the signal is passed through a level shifter to attenuate the PWM signal from +15V to +5V. As a result, S pulses between 0V and +5V.

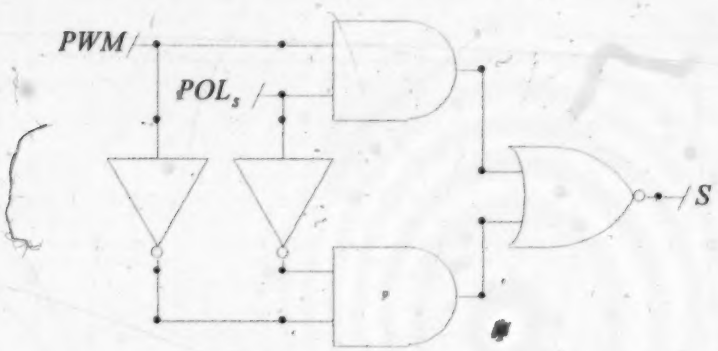


Figure 6.14: Actual switching signal applied to the single phase PWM boost rectifier

From figure 6.14, signal POL_s represents the polarity of the supply voltage and can be obtained using a comparator circuit which compares the feedback of the supply voltage with ground. When the supply voltage is higher than 0V, the comparator output is HIGH; when the supply voltage is negative, the comparator output is LOW. Similar to the PWM signal, the comparator output pulses between +15V and ground and as a result needs to be passed through a level shifter before it can be used with CMOS logic

circuitry. Figure 6.15 illustrates the circuit used for obtaining the polarity of the supply voltage.

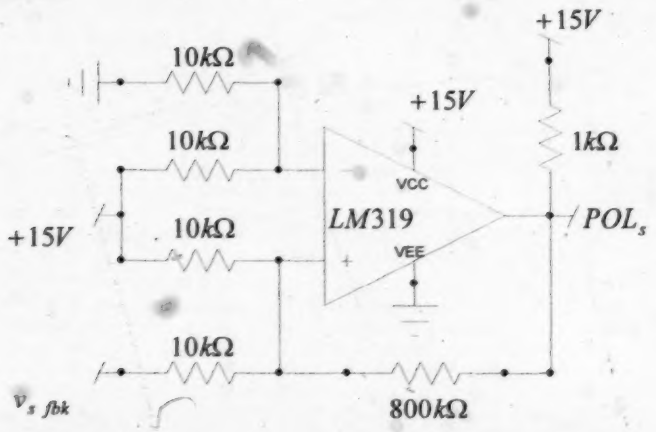


Figure 6.15: Polarity generator for the single phase supply voltage

Figure 6.16 illustrates the circuit used to generate the unipolar PWM signal for the obtaining the modulation depth signal utilized in the proposed single phase current control technique. Again, the PWM and POL_s are passed though a level shifter before being used with the logic circuitry. The gain of the differential amplifier is set to two in order to provide an output unipolar PWM signal that varies between ±10V.

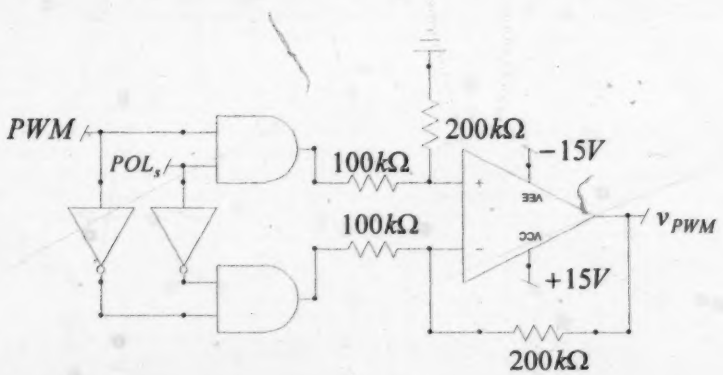


Figure 6.16: Unipolar PWM generator for the proposed single phase current control scheme

6.7 PWM Signal Generator for Three Phase Current Control Techniques

Three phase current control schemes discussed in this thesis work utilize the phase disposition PWM modulation strategy. The basic concept behind the generation of the PWM signals remains unchanged; however, the circuit utilizes two carrier signals and hence two separate PWM signals are created for each phase. Using the carrier signals generated in subsection 6.4.2, figure 6.17 shows the basic circuit for generating the upper (PWM_P) and lower (PWM_N) PWM signals for the three phase current control schemes.

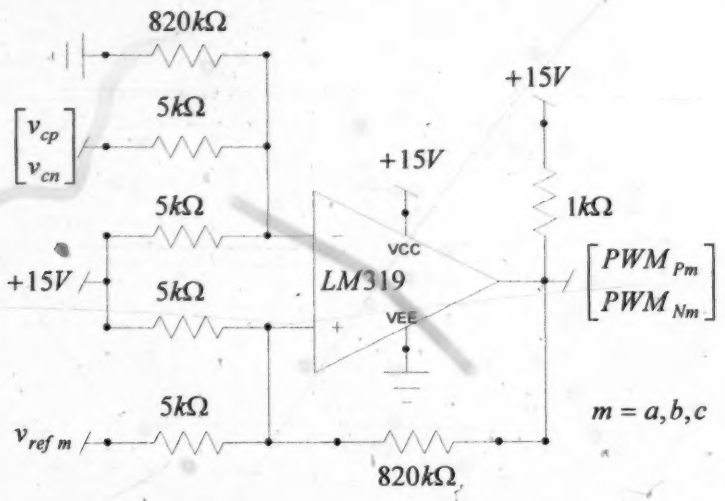
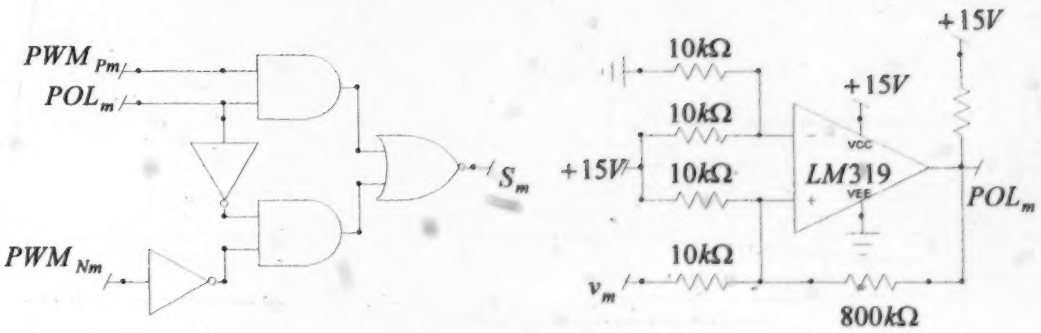


Figure 6.17: PWM signal generator for three phase current control techniques

Similar to §6.5, the effective hysteresis of this PWM generator is 45mV. For the stationary frame PI controller and the proposed 3-current controller, the actual switching signal S_m applied to the three phase PWM boost rectifier can be obtained by the using the following circuits. However, before the PWM signals are fed into the logic circuitry, they are passed through a level shifter to attenuate them from +15V to +5V. As a result, S_m pulses between 0V and +5V.



where v_m *is the line voltage feedback*
$m = a, b, c$

Figure 6.18: Actual switching signal applied to the three phase PWM boost rectifier for the stationary frame PI controller and 3-current controller

The modulation depth signals represent the sine wave voltage that is required at the rectifier input terminals to produce sinusoidal currents. As such, the bipolar PWM signals (PWM_P and PWM_N) are converted into unipolar PWM signals before generating the modulation depth signals.

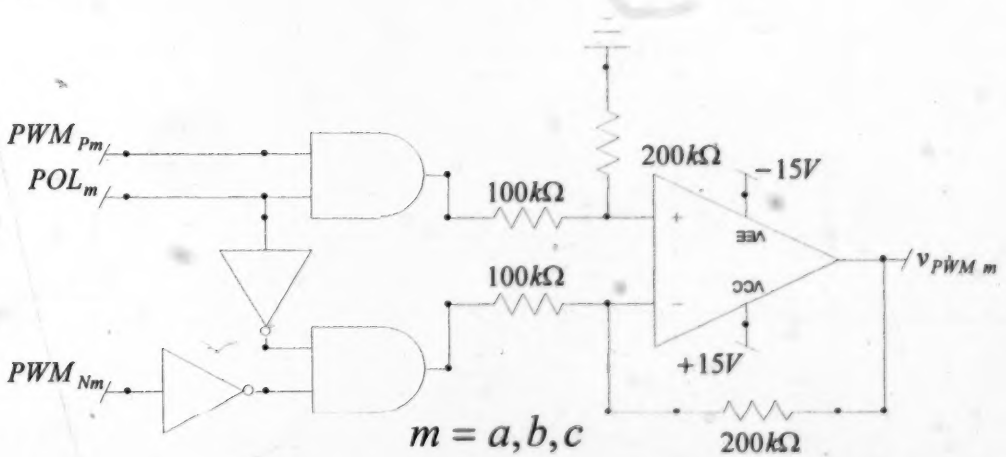


Figure 6.19: Unipolar PWM generator for the proposed three phase current control scheme

Figure 6.19 shows the circuit used to convert the bipolar PWM signals into unipolar PWM signals for the 3-current control scheme. The modified unipolar PWM signals for the proposed three phase current control scheme (see Chapter 3) can be obtained by using the circuit illustrated in figure 6.20. Considering only v_{PWMA} as an example:

$$v_{PWMA} = \frac{2}{3}v_{PWMa} - \frac{1}{3}v_{PWMb} - \frac{1}{3}v_{PWMc} \tag{6.44}$$

$$-\frac{1}{3}v_{PWMb} = \frac{R_5}{R_3}v_{PWMb} \Rightarrow R_3 = 3R_5 \tag{6.45}$$

$$-\frac{1}{3}v_{PWMc} = \frac{R_5}{R_4}v_{PWMc} \Rightarrow R_4 = 3R_5 \tag{6.46}$$

$$\frac{2}{3}v_{PWMa} = v_{PWMa}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_3 // R_4 + R_5}{R_3 // R_3}\right) = v_{PWMa}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{5}{3}\right)$$
$$\Rightarrow R_2 = \frac{2}{3}R_1 \tag{6.47}$$

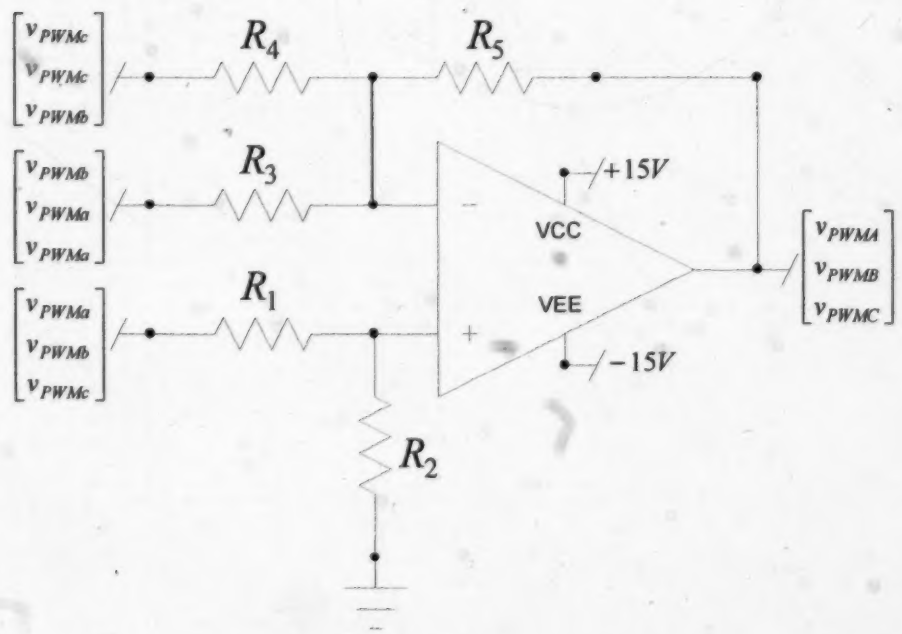


Figure 6.20: Modified PWM feedback signal generator

Using equations (6.45), (6.46), and (6.47):

$$\text{Let } \underline{R_1 = 51k\Omega} \Rightarrow \underline{R_2 = 100k\Omega}$$
$$\text{Let } \underline{R_5 = 15k\Omega} \Rightarrow \underline{R_3 = R_4 = 100k\Omega} \qquad (6.48)$$

Analyzing the circuit for v_{PWMB} and v_{PWMC} yields the same resistor values.

6.8 Switching Logic for the 2-Current Control Technique

The 2-current control scheme uses Table 3-III and Table 3-IV (see Chapter 3, Section 3.5) to generate the actual PWM switching signals applied to the three phase PWM boost rectifier. Tables 3-III and 3-IV are modified to include the PWM signals generated by the circuit illustrated in figure 6.17. The modified switching patterns are represented in Table 6-I and 6-II.

Table 6-I: Switching Pattern for Star-Connected PWM Boost Rectifier

60° Periods	Star		
	S_a	S_b	S_c
330°-30°	ON	$\overline{PWM_{Nb}}$	PWM_{Pc}
30°-90°	PWM_{Pa}	$\overline{PWM_{Nb}}$	ON
90°-150°	PWM_{Pa}	ON	$\overline{PWM_{Nc}}$
150°-210°	ON	PWM_{Pb}	$\overline{PWM_{Nc}}$
210°-270°	$\overline{PWM_{Na}}$	PWM_{Pb}	ON
270°-330°	$\overline{PWM_{Na}}$	ON	PWM_{Pc}

Table 6-II: Switching Pattern for Delta-Connected PWM Boost Rectifier

60° Periods	Delta		
	S_{ab}	S_{bc}	S_{ca}
330°-30°	$\overline{PWM_{Nb}}$	OFF	PWM_{Pc}
30°-90°	OFF	$\overline{PWM_{Nb}}$	PWM_{Pa}
90°-150°	PWM_{Pa}	$\overline{PWM_{Nc}}$	OFF
150°-210°	PWM_{Pb}	OFF	$\overline{PWM_{Nc}}$
210°-270°	OFF	PWM_{Pb}	$\overline{PWM_{Na}}$
270°-330°	$\overline{PWM_{Na}}$	PWM_{Pc}	OFF

For proper operation of the 2-current control scheme, pulses corresponding to each 60° interval need to be generated. There are several ways this task can be accomplished; however, the simplest method for obtaining the pulses for each 60° period uses the feedback of the line-line voltage and is illustrated in figure 6.21.

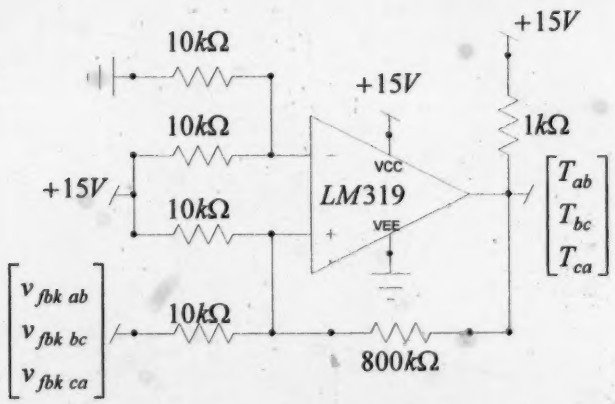


Figure 6.21: Generating the pulse template

The pulse template generator generates a HIGH pulse whenever the line-line feedback voltage is greater than 0V; the output of the pulse generator is LOW whenever the line-line feedback voltage is below 0V. Individual pulses for each 60° period can be

easily generated by using CMOS logic ICs and the above pulse templates. The pulse equations can be expressed as follows:

$$\begin{aligned}
&330°-30° \Rightarrow P_1 = T_{ab} \bullet T_{ca} \\
&30°-90° \Rightarrow P_2 = \overline{T_{bc}} \bullet \overline{T_{ca}} \\
&90°-150° \Rightarrow P_3 = T_{ab} \bullet T_{bc} \\
&150°-210° \Rightarrow P_4 = \overline{T_{ab}} \bullet \overline{T_{ca}} \\
&210°-270° \Rightarrow P_5 = T_{bc} \bullet T_{ca} \\
&270°-330° \Rightarrow P_6 = \overline{T_{ab}} \bullet \overline{T_{bc}}
\end{aligned} \qquad (6.49)$$

Using equation (6.49) and Tables 6-I and 6-II, the switching pattern for the star-connected and delta-connected bidirectional switch PWM boost rectifier can be expressed in the following expression:

$$\begin{aligned}
S_a &= (P_2 + P_3) \bullet \mathrm{PWM_{Pa}} + (P_5 + P_6) \bullet \overline{\mathrm{PWM_{Na}}} \\
S_b &= (P_4 + P_5) \bullet \mathrm{PWM_{Pb}} + (P_1 + P_2) \bullet \overline{\mathrm{PWM_{Nb}}} \\
S_c &= (P_1 + P_6) \bullet \mathrm{PWM_{Pc}} + (P_3 + P_4) \bullet \overline{\mathrm{PWM_{Nc}}} \\
S_{ab} &= P_3 \bullet \mathrm{PWM_{Pa}} + P_4 \bullet \mathrm{PWM_{Pb}} + P_6 \bullet \overline{\mathrm{PWM_{Na}}} + P_1 \bullet \overline{\mathrm{PWM_{Nb}}} + P_2 + P_5 \\
S_{bc} &= P_5 \bullet \mathrm{PWM_{Pb}} + P_6 \bullet \mathrm{PWM_{Pc}} + P_2 \bullet \overline{\mathrm{PWM_{Nb}}} + P_3 \bullet \overline{\mathrm{PWM_{Nc}}} + P_1 + P_4 \\
S_{ca} &= P_1 \bullet \mathrm{PWM_{Pc}} + P_2 \bullet \mathrm{PWM_{Pa}} + P_4 \bullet \overline{\mathrm{PWM_{Nc}}} + P_5 \bullet \overline{\mathrm{PWM_{Na}}} + P_3 + P_6
\end{aligned} \qquad (6.50)$$

The switching logic presented in equation (6.50) can be easily implemented using CMOS based logic circuitry. Note that the actual PWM switching signals applied to the star-connected and delta-connected bidirectional switch PWM boost rectifiers are in fact: $\overline{S_a}, \overline{S_b}, \overline{S_c}, \overline{S_{ab}}, \overline{S_{bc}}$, *and* $\overline{S_{ca}}$. Figure 6.22 shows the circuit used to convert the bipolar PWM signals into unipolar PWM signals for the 2-current control scheme. Both star-connected and delta-connected configurations utilize the same bipolar PWM signal feedback. This circuit uses the phase voltage polarity signal POL_m generated by the circuit in figure 6.18. The differential amplifier gain is set to two since the unipolar PWM feedback signals are required to vary between ±10V.

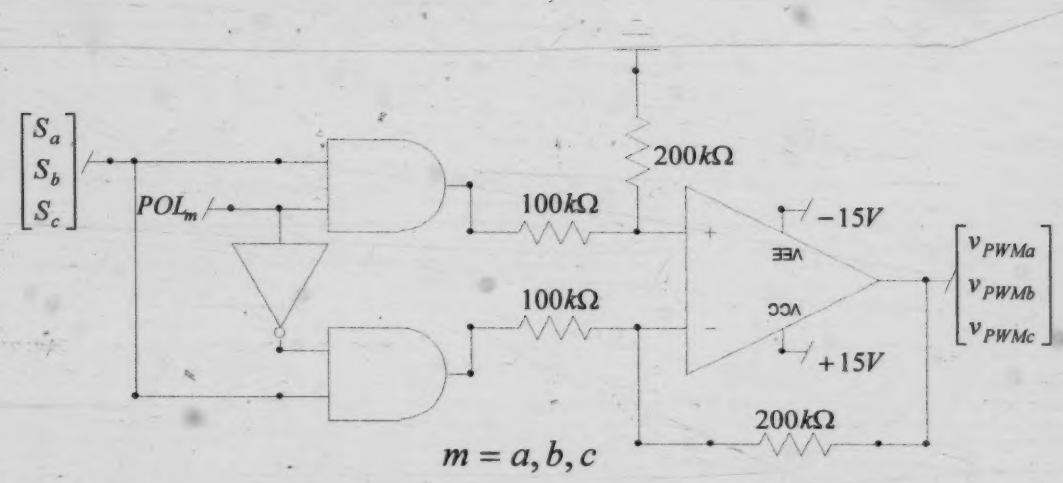


Figure 6.22: Unipolar PWM generator for the 2-current control scheme

6.9 Modulation Depth Signal Generation Using Low-pass Butterworth Filters

The modulation depth signal represents the sinusoidal signal which must be present at the rectifier input terminals to produce a sinusoidal current. From Chapter 3, it is clear that the average of the unipolar PWM signal is equivalent to the modulation depth signal. Furthermore, it was concluded that averaging the PWM signal via a second order low-pass Butterworth filter yields similar performance as the sample and hold technique; sample and hold provides the fastest means of averaging the PWM signal at the cost of higher complexity. A simple second order low-pass Butterworth filter with a unity gain provides exceptional performance with a balance between fast averaging and small phase shifts. Figure 6.23 illustrates a single opamp 2nd order low-pass Butterworth filter with an f_{20dB} determined by the carrier frequency.

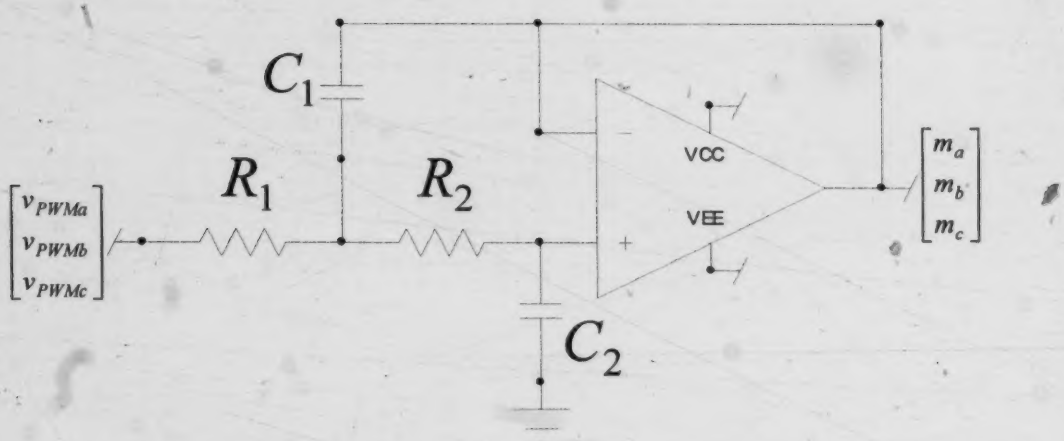


Figure 6.23: A unity gain 2nd order lowpass Butterworth filter

The -20dB attenuation frequency f_{20dB} is the frequency where the output signal magnitude is $1/10^{th}$ of the input signal magnitude. Using the relationship $f_{3dB} = 0.318 \times f_{20dB}$, the filter components for various f_{20dB} values are given as follows:

$$f_{20dB} = 60Hz \rightarrow f_{3dB} = 19.1Hz \Rightarrow R_1 = 75k\Omega, R_2 = 284k\Omega, C_1 = 100nF, C_2 = 33nF$$
$$f_{20dB} = 5kHz \rightarrow f_{3dB} = 1.6kHz \Rightarrow R_1 = 10k\Omega, R_2 = 33k\Omega, C_1 = 10nF, C_2 = 3.3nF$$
$$f_{20dB} = 10kHz \rightarrow f_{3dB} = 3.19kHz \Rightarrow R_1 = 4.7k\Omega, R_2 = 16.5k\Omega, C_1 = 10nF, C_2 = 3.3nF$$
$$f_{20dB} = 15kHz \rightarrow f_{3dB} = 4.78kHz \Rightarrow R_1 = 3k\Omega, R_2 = 11k\Omega, C_1 = 10nF, C_2 = 3.3nF$$
$$f_{20dB} = 20kHz \rightarrow f_{3dB} = 6.37kHz \Rightarrow R_1 = 2.2k\Omega, R_2 = 8.2k\Omega, C_1 = 10nF, C_2 = 3.3nF$$

6.10 Summary

Implementation of the single phase and three phase current control schemes using low cost, discrete analog and digital electronic components was investigated. Several analog circuits were designed and tested; key design equations necessary for calculating the component values were also presented. The analog nature of the design yields a simple and cost effective control scheme while providing good control performance with high stability.

Chapter 7 Analysis of Experimental Results

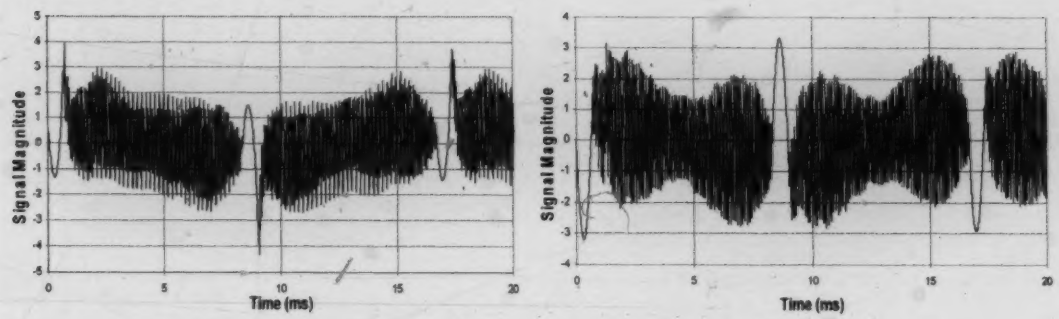
Experimental results for the single and three phase current control schemes are presented. To verify the quality of the current control, the performance of the single and three phase control techniques is examined under stead-state conditions by analyzing the experimental data. The current controllers are implemented using the discrete electronic circuitry detailed in Chapter 6 and are applied to a single/three phase PWM boost rectifier in order to study their behaviour. Experimental results indicate that the proposed single phase control scheme yields stable steady-state operation with a zero average current error and an inherent tolerance to the presence of DC offsets in the control signals when compared to a similarly tuned PI current controller. Similarly, analysis of the experimental results indicates the proposed three phase current control technique and 2-current control technique yield stable steady-state operation with a high tolerance to system disturbances such as DC offset voltages when compared to a similarly tuned PI current controller in the stationary reference frame.

7.1 Experimental Results for the Single Phase Current Control Schemes

In this section, experimental results for a proportional-integral current controller and the proposed single phase PWM feedback current controller are presented. A single phase PWM boost rectifier, with a supply voltage of 120 V and an effective line inductance of 5 mH, is used to study the behaviour of the PI current controller and the proposed single phase current control schemes; experimental results are obtained for full power operation (i.e. I_s = 10 A_{peak} and V_{DC} = 200 V) with a 5 kHz carrier frequency. The operating conditions for the current controllers are chosen as to allow for the implementation of a low power prototype; commercial and industrial applications such as active filters and VFDs would require the controller to operate at voltages significantly higher than those available in a laboratory setting. Furthermore, the controllers are operated at full power to indicate their performance under the worse case scenario. It is quite feasible to operate the current controllers at half the supply voltage and power; however, at very low input voltages, accurate control of the line current is lost.

Both control schemes are tuned to provide a zero average current error. For the single phase PI current control scheme, $K_i = f_c$. For the proposed PWM feed back

technique, $f_{20dB} = f_c$. The experimental data is obtained using a TSD 420 oscilloscope and Tekvisa data acquisition software.

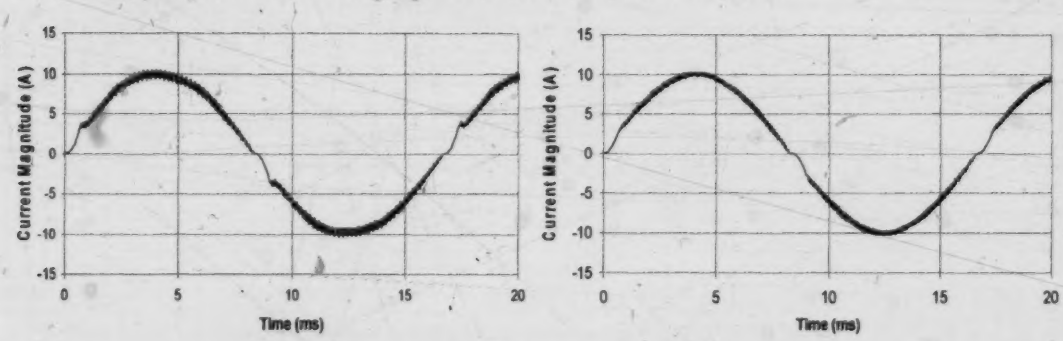


(a) PI Current Control Scheme (b) Proposed Current Control Scheme

Figure 7.1: Experimental results: single phase -$K_p i_{error}$

Figure 7.1 illustrates the scaled current error signals for the single phase PI and the proposed single phase current control schemes. Comparing figure 7.1 with figure 4.2 (a) and figure 4.6 (a), yields similarities between the simulation response and the experimental response of the two controllers. Both current control schemes yield a small average current error while maintaining the magnitude of the high frequency ripple between 5 $V_{peak\text{-}peak}$.

Figure 7.2 (a)-(b) illustrates the steady-state supply current waveform over one fundamental cycle for both single phase current control schemes.



a) PI Current Control Scheme (2.1% THD) (b) Proposed Current Control Scheme (1.9% THD)

Figure 7.2: Experimental results: single phase supply current

Both current control schemes experience large current errors at the beginning of each supply half cycle; these large current errors can be attributed to the *di/dt* of the supply inductance and are independent of the control schemes. As such, these regions of large error cannot be controlled directly by the current controllers; however, these low frequency distortions can be reduced by lowering the size of the line inductor. Experimental data indicate that the PI current control scheme experiences a larger current error than the proposed current control scheme and as a result, the PI current controller experiences larger current overshoots at the beginning of each supply half-cycle. Both control schemes yield UFPF operation. Figure 7.3 shows the modulation depth signal for the proposed single phase current control scheme. Figure 7.4 illustrates the behaviour of the PI current controller and the proposed PWM feedback current control technique to DC offset conditions.

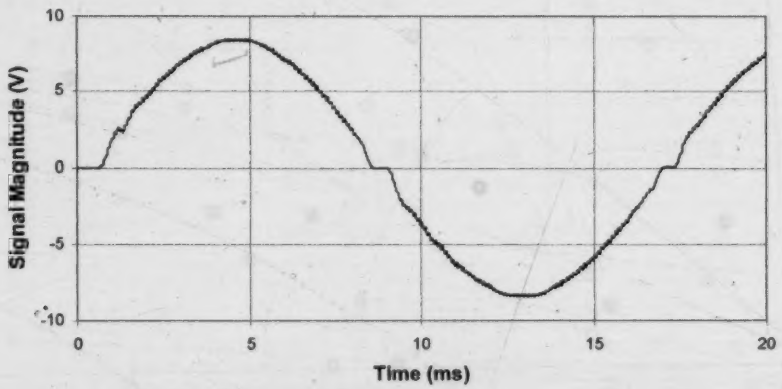
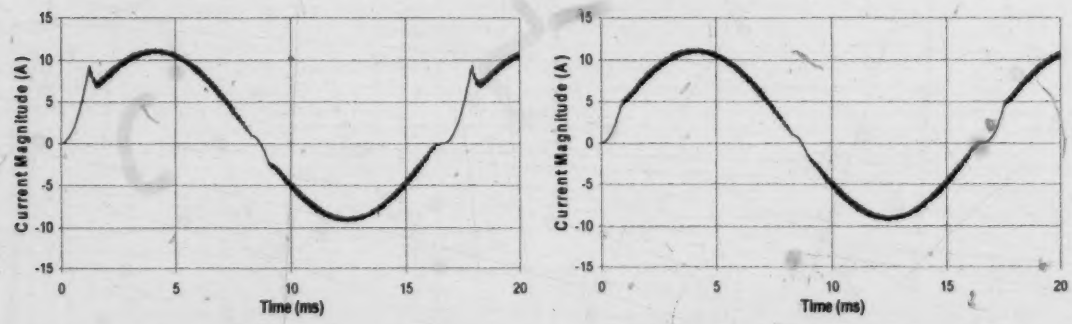


Figure 7.3: Proposed single phase current control scheme: modulation depth signal



a) PI Current Control Scheme (b) Proposed Current Control Scheme

Figure 7.4: Experimental results: behaviour of the single phase current control schemes under 1 V DC offset

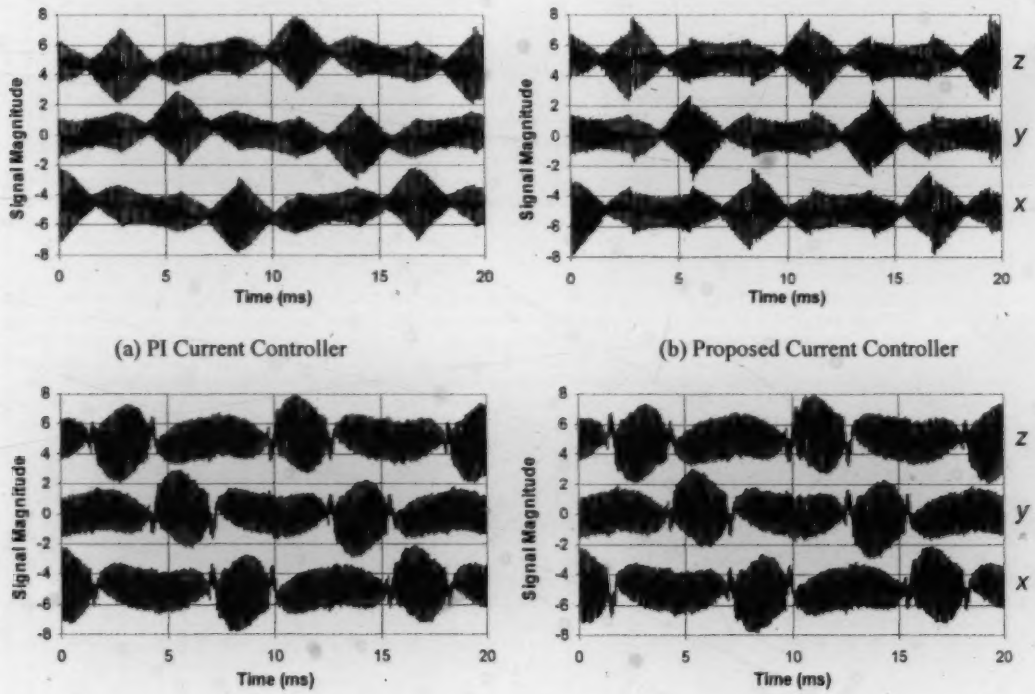
In order to test the ability of the control schemes to tolerate DC offsets in the system, a 1 V DC offset is introduced in the current reference signal (i_{ref}). From figure 7.4, it is clear that the presence of a DC offset in the current reference signal leads to large current overshoots in the PI current control scheme as opposed to the proposed PWM feedback current control technique. Experimental results depicted in figure 7.4 are clear evidence that the proposed single phase current control scheme displays superior tolerance to offset disturbances in the system than the industry standard PI current controller.

7.2 Experimental Results for the Three Phase Current Control Schemes

Experimental results for the stationary frame PI current controller, the proposed 3-current PWM feedback current control scheme, and 2-Current control scheme are presented. Each control scheme is applied to a three phase PWM boost rectifier with an input voltage of 120 V and an effective line impedance of approximately 2.5 mH. The rectifier is operated at full power with 10 A_{peak} line current currents and 300 V DC link voltage. The carrier frequency for the stationary frame PI controller and the proposed current control scheme is set at 10 kHz; carrier frequency for the 2-current control schemes is set at 15 kHz. Again, the operating conditions are selected as to facilitate the implementation of the controllers in a laboratory environment. Industrial applications would require these controllers to work on significantly higher operating conditions. All three phase current controllers are tuned to provide similar performance to facilitate comparison between the techniques. The PI compensators are designed for an integral gain equal to the carrier frequency. The proposed 3-current control scheme utilizes $f_{20dB} = 2f_c$ while the 2-current control schemes utilize $f_{20dB} = f_c$. The experimental data is obtained using a TSD 420 oscilloscope and Tekvisa data acquisition software.

Experimental results illustrating the steady-state current errors of the different three phase current control schemes are presented in figure 7.5. Experimental steady-state current error signals for each current control technique are in close resemblance to their simulation counterparts. The presence of a fundamental component on the PI current control scheme is minimal (figure 7.5 (a)) and can be attributed to the tolerances of the capacitor values used to obtain the integral gain portion of the PI compensator.

The proposed three phase current control scheme and the 2-current control techniques both yield a zero average current error. The peak-to-peak ripple of the scaled current error signal is limited within 5 $V_{peak\text{-}peak}$ for all control schemes.



(a) PI Current Controller (b) Proposed Current Controller

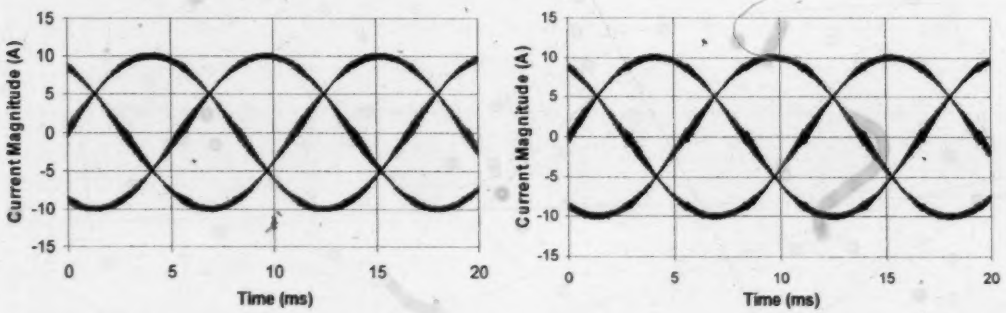
(a) 2-Current Controller (Star) (b) 2-Current Controller (Delta)

Key: x - Kpi_{errora} y - Kpi_{errorb} z - Kpi_{errorc}

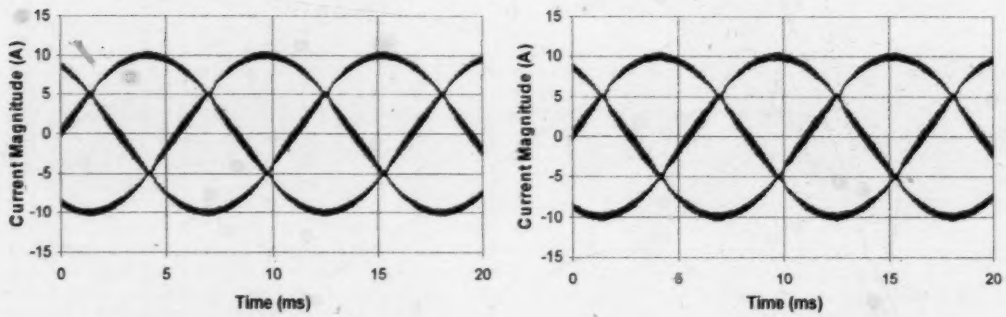
Figure 7.5: Offset experimental waveforms: comparison of three phase steady-state current error signals

Figure 7.6 illustrates the steady-state line current waveforms for the three phase current control schemes over one fundamental cycle. Again, experimental waveforms closely resemble results obtained via computer simulations. Despite the presence of a fundamental component in the current error signals, the stationary frame PI current control scheme maintains good current control. The proposed three phase current controller and the 2-current control schemes demonstrate excellent current wave-shaping capabilities with minimal high frequency distortions at zero crossovers. The presence of

low frequency distortion at phase crossover points is observed for the 2-current control schemes; this is consistent with the results obtained via simulations. All current control schemes yield a unity fundamental power factor.



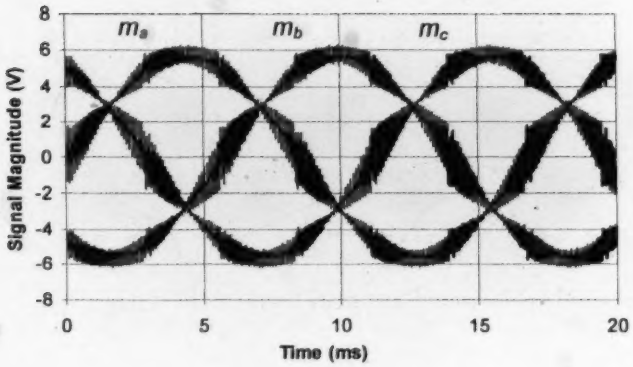
(a) PI Current Controller (3.3% THD) (b) Proposed Current Controller (3.0% THD)



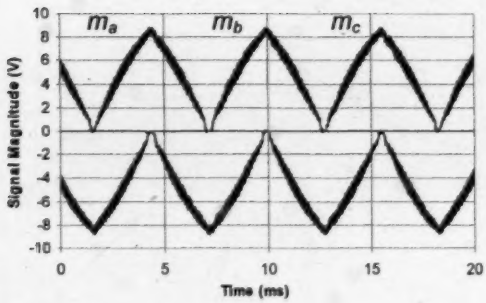
(a) 2-Current Controller (Star – 2.9% THD) (b) 2-Current Controller (Delta – 2.9% THD)

Figure 7.6: Experimental results: three phase supply current waveforms

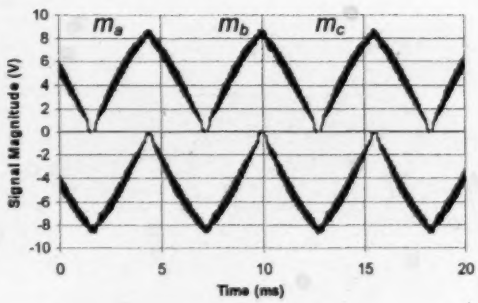
The modulation depth signals for the proposed three phase current control scheme and the 2-current control scheme are presented in figure 7.7.



(a) Proposed Current Controller



(b) 2-Current Controller (Star)

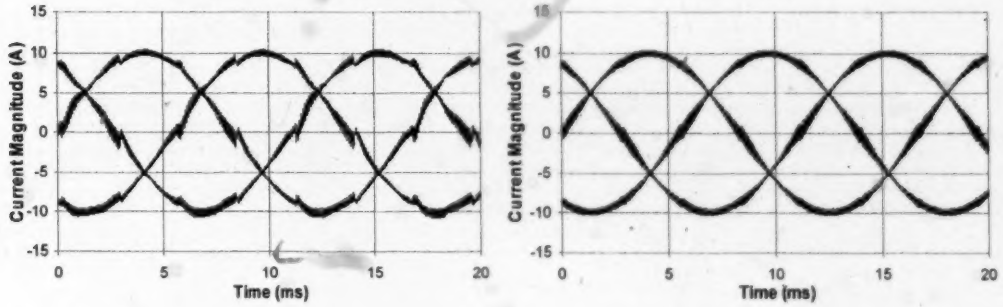


(c) 2-Current Controller (Delta)

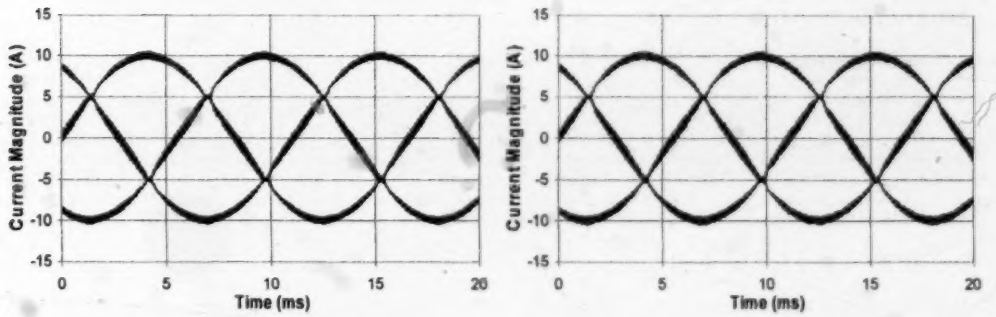
Figure 7.7: Experimental results: three phase modulation depth signals

Figure 7.8 illustrates the behaviour of the three phase current control techniques to DC offset conditions. The behaviour of the three phase current control is examined under system offset disturbances. By introducing a 100 mV DC offset in the current reference signals, the tolerance of the control scheme to offset voltages is observed. From figure 7.8, it is apparent that the stationary frame PI current control responds poorly to offsets in the control signals. Presence of a DC offset in the current reference signal leads to general instability and large current overshoots in the PI control scheme which degrades the quality of the control. Such instability and overshoots are not observed in the proposed 3-current control and 2-current control schemes. This leads to the conclusion that the proposed three phase current control scheme and the 2-current control scheme provide a more robust control strategy with a significantly higher tolerance to

system disturbances such as offset voltages in the control signals than the similarly tuned stationary reference frame PI current controller.



(a) PI Current Controller (b) Proposed Current Controller



(a) 2-Current Controller (Star) (b) 2-Current Controller (Delta)

Figure 7.8: Experimental results: behaviour of the three phase current control schemes under 100 mV DC offset

7.3 Summary

Experimental results for the single and three phase current control schemes are presented and compared to evaluate the behaviour and quality of control provided by each scheme. Both single phase and three phase experimental results are consistent with those obtained via computer simulations. Experimental data, along with the simulation results obtained earlier, confirm that the proposed single and three phase current control schemes yield stable steady-state operation with zero average current error and a high tolerance to the presence of DC offsets in the control signals when compared with a similarly tuned single and three phase PI current controller, respectively.

Chapter 8 Conclusions and Future Work

Harmonic distortions in utility power supplies and the deterioration of power factors due to non-linear loads can be considered to be a form of electrical pollution which can have dire consequences on industrial equipment and processes. Such effects can range from spurious operation of equipment to reduced efficiency of the entire power system. Hence there is a recognized demand for rectifiers with high power factor and low current harmonic distortions. Consequently, extensive effort is being devoted towards the development of effective control strategies for switch-mode utility rectifiers. Current controlled PWM rectifiers have distinct advantages over conventional rectifiers such as near sinusoidal supply currents with a unity fundamental power factor and bi-directional power flow.

This thesis focuses on the analysis, design and implementation of a novel unipolar pulse width modulated (PWM) current control technique for single and three phase unity fundamental power factor (UFPF) utility rectifier topologies.

8.1 Thesis Contributions

The performance of a converter system is highly dependant on the current control scheme being utilized. In general, a current control strategy must provide ideal tracking by allowing no phase or amplitude errors, fast transient response to provide high system dynamics, and a constant switching frequency to ensure safe operation of semiconductor devices. Existing control strategies can achieve low harmonic distortions while maintaining a unity fundamental power factor. The existing current control techniques often fall into two categories: control schemes derived from hysteresis-band current control and control schemes which utilize a fixed frequency carrier signal. Hysteresis-based current control schemes exhibit exceptional control performance and make it easy to obtain a small current error; however, the switching frequency is highly dependant on system parameters and can vary with the supply voltage. On the other hand, carrier-based control schemes provide a fixed switching frequency but require complex circuitry to obtain a small current error.

The proposed single and three phase current control schemes and the 2-current control technique combine the advantages of both the hysteresis based current control and carrier-based current control schemes. In all cases, the modulation depth signals are generated by taking the average of the PWM signals using 2^{nd} order low-pass Butterworth filters. Together with their respective current error signals, the modulation depth signals are used to produce the voltage reference signals necessary for PWM modulation. As a result, natural changes in the ramping rate of the current error signals yields an automatic change in the average of the PWM signals. This allows the controller to maintain a zero average current error while providing a fixed switching frequency.

The performance of the proposed single phase and three phase current control schemes is examined in steady-state and during transients using simulation results. Single and three phase PI current control schemes are also simulated to provide a comparison base between the proposed control schemes and the industry standard PI current controllers. To test the robustness of the different controllers, the behaviour of the proposed control schemes and the PI current controllers is examined under system disturbances such as DC offset voltages. Simulation results indicate that the proposed single and three phase current control schemes, as well as the 2-current control technique, yield stable steady-state operation with zero average current error, quick transient responses to step changes in the demand current with minimal current overshoots, and an inherent tolerance to the presence of DC offsets in the control signals when compared to a similarly tuned single and three phase PI current control scheme, respectively.

Analog realizations of the current controllers are developed and implemented based on theoretical and simulation results. The proposed current control schemes are designed for implementation with low cost, discrete analog and digital electronic components. In order to study the performance of the control schemes, the proposed current controllers and the PI current controllers are applied to single phase and three phase PWM boost rectifiers, respectively. The experimental results demonstrate excellent performance of the proposed control schemes and present good agreement between the simulations and experiments.

8.2 Future Work

This work has provided a key step forward towards the development of hybrid type current control schemes for industrial applications. Analog circuitry is prone to component value variations and offset voltages which prevent the development of an accurate control scheme; a digital signal processor (DSP) realization of the proposed current control schemes is feasible and would serve to eliminate these limitations posed by the analog circuitry. Further studies into the behaviour of the proposed schemes under heavy voltage and phase imbalances for three phase systems would also be considered a valuable course of study.

Although the proposed current control schemes are designed and tested on single and three phase PWM boost rectifier topology, slight modifications to the switching signals would allow these controllers to operate with traditional bridge rectifier topologies and single/three phase inverters. This can extend the applicability of the proposed current controllers.

Typically, industrial applications of PI current controllers incorporate measures to limit the integral term from becoming excessively large during a transient response (anti-windup). The goal of an anti-windup circuit is to counteract the integration of the controller by bounding the integration term within a certain limit. The presence of anti-windup measures minimizes the overshoots commonly encountered during a transient response when using a PI current control scheme. The PI current controllers implemented in this research work did not incorporate any anti-windup measures and as such, it needs to be the focus for future work.

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